SIEMENS

Intelligent Displays

Data Book 1984/85

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Intelligent Displays

Intelligent displays are LED alphanumeric displays with built-in CMOS decoder, multiplexer, memory, and driver. They easily interface with any microprocessor bus and feature a compact design that allows a wide variety of design configurations.

The first "Intelligent Display", the DL 1416, was announced in May 1977. Since that time, many new versions have been introduced, ranging in character height from 2.8 mm for the DL 1414 and DL 1814 to 4.1 mm for the DL 1416 and DL 2416, up to 4.3/2.5 mm upper and lower-case for the DL 3422, 5.7 mm for the DL 3416 and 17.3 mm for the 5×7 dot matrix displays DLO 7135 (orange) and DLG 7137 (green).

LED intelligent displays have become increasingly popular since their introduction. Consider them for your application and take advantage of these features:

- Totally self-contained display peripherals that minimize design time
- Compatibility with microprocessor bus systems
- Single 5 V supply operation
- CMOS logic, TTL-compatible
- No noticeable degradation, a life expectancy that exceeds 250,000 hours
- Bright, high-contrast LED technology
- Highly compact, flat package
- Easily end-stackable for expandable message lengths
- Brightness coded for easy matching
- Direct random access at any location

Guidelines for handling and using intelligent displays

Since we began manufacturing the intelligent displays in 1978, several questions concerning their use have arisen.

This section is a guide for considerations in design and handling of this product.

Intelligent displays are one, four, or eight-digit display modules, having a 16, 17, or 22 segment font or a 5×7 dot matrix, and an on-board CMOS integrated circuit driver. The CMOS chip provides segment decoding, segment driving, multiplexing and memory for easy interfacing with most microprocessors.

System design considerations

The practical circuit design (i.e. design of PCB, etc.) should be such that **the voltage to any input is not allowed to exceed the voltage at the power supply inputs** (i.e. GND $< V_{IN} < V_{CC}$). If these conditions are not kept, then malfunction or – at worst – device destruction may occur. The most frequent cause for this phenomenon is circuit noise due to noise on the input leads and transient power supply changes.

Good circuit layout

The principles of good circuit layout resemble those of every logic circuitry; the tolerances of MOS circuitry, however, are much lower than those of bipolar logic. The most important principle is to keep the lead length from the output of one device to the input of another as short as possible, hence reducing the coupling effect between input signals.

Buffering

The second most common deviation from good design practice is the use of parallel tracking. PCB design which allows an interconnection track running in parallel should therefore be avoided. This is particularly true if one of the tracks is a power supply bus; then the fluctuations of the power supply current can cause inductively coupled changes in the input track. Possibly, the worst example of parallel tracking is the ribbon cable: it is physically neat and convenient, but can be electrically destructive for MOS circuits.

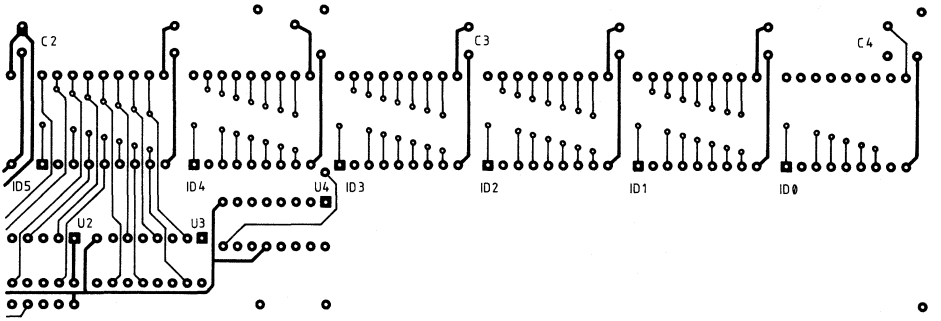
It is, however, often necessary to use a ribbon cable between the display assembly and the display board because of the very nature of the intelligent displays. In such cases **use a TTL buffer for each used input if the cables exceed 15 cm** (6 inches). This particularly applies to noisy systems which have motors, relays, etc. The buffers must be on the display end of the cable, thus keeping a minimum distance between their outputs and the display inputs. Long cables can be a poor transmission line for high-speed pulses. Line drivers, line receivers, or schmitt trigger gates may, therefore, be required for steep pulse slopes.

Voltage transients

It has become common practice to liberally provide digital systems with 0.01 μF bypass capacitors. For intelligent displays, the emphasis is on adequate decoupling. Like other CMOS circuits, the intelligent display controller chip has very low power consumption.

The usual 0.01 µF capacitors would therefore be adequate for the IC but not for the LEDs. In some modes of operation, the module itself can use up to 100 mA (multiplexed). In order to prevent power supply transients, capacitors with low inductance and high frequencies are required. This suggests a solid tantalum or ceramic disk for high-frequency bypass. For larger displays the bypass capacitors should evenly be distributed, keeping the capacitors as close to the power pins as possible.

Do not rely on existing on-board decoupling, use a 10 µF and 0.01 µF capacitor for every 3 or 4 intelligent displays to decouple the displays themselves (refer to figure).



The figure illustrates a pertinent PCB layout for an assembly of DL 2416 intelligent displays. The capacitors are evenly spaced and close to the displays with sufficient space for additional capacitors should the system need them.

Functional limitations

Several parameters in the intelligent display data sheet which may affect your design will be emphasized once more. Even if not keeping these parameters may not be destructive, it may affect reliability and/or functional operation (refer also to the data sheets).

The following should be considered:

- the period of time all cursors may be lit should be 1 minute max. (does not apply to DLX 713*)
- the timing parameters for 25 °C will increase with rising temperature
- the timing parameters will increase with increasing V_{CC}.

Manufacturing Considerations

Handling

The static voltages generated by friction with modern synthetic materials (i.e. carpets, clothing, device carriers, etc.) are often measured in thousands of volts. Although there is usually little energy in these static charges, that energy is sufficient to cause destruction to MOS circuitry if applied between circuit inputs. Input protection diodes can minimize the vulnerability of the circuits, but there is a limit to their protecting capabilities. Under certain conditions, static charges may exceed that limit.
The most effective protection is to avoid the generation of static charges. If they are, however, inevitable, the charge must be prevented from coming into contact with the device pins.

1. Avoid touching the pins; handle the body only.
2. Keep the devices in anti-static tubes or conductive material when transporting.
3. Use a conductive and grounded working area (conductive flooring, conductive work benches, individual wrist straps, etc.).

Brightness codes

Display uniformity is a concern if two or more displays are in one system. A letter code (A to H) for 8 brightness groups has therefore been adopted to obtain a uniform display. It is recommended a single letter code be used per system. As this may be difficult due to yield and delivery, adjacent codes (i.e. D with E, E with F) may be used. Jumping over a code (i.e. D with F) may be noticed by most critical observers.

Soldering

Owing to the plastic housing of the intelligent displays, it is necessary to control the solder temperature, soldering time, and solder distance.

A maximum of 260 °C for 3 seconds at a distance of greater than 1.59 mm is required.

In case of wave soldering, moreover, the temperature of intelligent displays' packages is not allowed to exceed 70 °C.

Cleaning

The cleaning process of intelligent displays is the crucial factor for maintaining the optical efficiency of the plastic housing. The solvent that cannot be used on the intelligent display product is alcohol. Alcohol will attack the lens material causing cracking, crazing, and destruction of the clear optical properties of the lens.

Suitable cleaning agents are chlorinated hydrocarbons (Acetone, 1.11 Trichloraethane, etc.) or freon TF, freon TA, or warm DI water.

One note of caution: do not use a freon solvent without first finding out the chemical composition. Some manufacturers use some forms of alcohol as an additive, so beware.

The DLX 713* should only be cleaned in water, isopropyl alcohol, freon TF, or TE (or equivalent).

Summary of Types

Display modules

Type	Character height	Color	Viewing angle	Segments per digit	Page
DL 1414	2.8 mm	red	±40 degrees	16 plus decimal	11
DL 1416	4.1 mm	red	±20 degrees	16	28
DL 1814	2.8 mm	red	±33 degrees	16 plus decimal	54
DL 2416 DL 2416 H	4.1 mm	red	±50 degrees	16 plus decimal	60
MDL 2416 MDL 2416 B	3.81 mm	red	±50 degrees	16 plus decimal	68
DL 3416 DL 3416 H	5.7 mm	red	±40 degrees	16 plus decimal	88
DL 3422	4.3 mm 2.5 mm	red	±50 degrees	22	96
DLO 7135 DLG 7137	17.3 mm	orange green	±75 degrees	5×7 dot matrix	104

Display assemblies

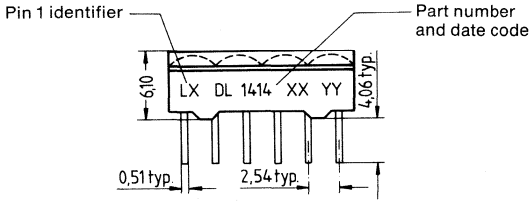
Type	Character height	Color	Display length	Remarks	Page
IDA 1414–16–1 IDA 1414–16–2	2.8 mm	red	16 digits	buffered non buffered	120
IDA 1416–32	4.1 mm	red	32 digits	Other lengths upon request	127
IDA 2416–16 IDA 2416–32	4.1 mm	red	16 digits 32 digits		134
IDA 3416–16 IDA 3416–20 IDA 3416–32	5.7 mm	red	16 digits 20 digits 32 digits		141
IDA 3422–16 IDA 3422–20	4.3/2.5 mm	red	16 digits 20 digits		149
IDA 7135–16 IDA 7135–20 IDA 7137–16 IDA 7137–20	17.3 mm (dot matrix)	orange green	16 digits 20 digits 16 digits 20 digits		157

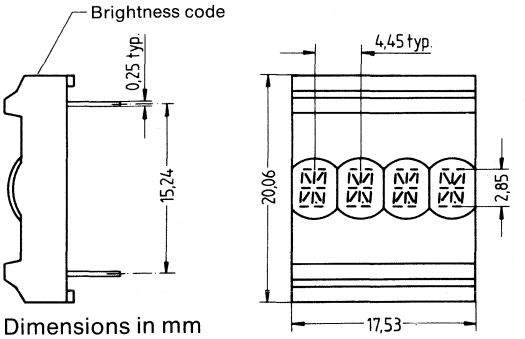
Alphanumeric intelligent display with memory, decoder, and driver.
2.8 mm, red, 4 digits, 17 segments

Features

- 2.8 mm high, magnified monolithic characters
- Wide viewing angle, ±40 degrees
- Close vertical row spacing, 20.1 mm
- Rugged solid plastic encapsulated package
- Fast access time, 450 ns
- Compact size for hand-held equipment
- Built-in memory
- Built-in character generator
- Built-in multiplex and LED drive circuitry
- Direct access to each digit independently and asynchronously
- TTL compatible, 5 V power supply
- 17th segment for improved punctuation marks
- Low power consumption, typically 10 mA per character
- Intensity coded for display uniformity
- End-stackable, 4 character package

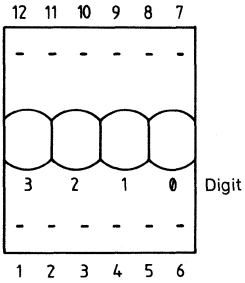
Type	Ordering code
DL 1414	Q68000–A5559–F114





Dimensions in mm

Tolerance ±0.25 mm, unless otherwise specified



Pin configuration (top view – display side)

Pin	Function		Pin	Function	
1	D5	Data input	12	D6	Data input (MSB)
2	D4	Data input	11	D3	Data input
3	$\overline{WR}$	Write	10	D2	Data input
4	A1	Digit select	9	D1	Data input
5	AØ	Digit select	8	DØ	Data input (LSB)
6	V_{CC}	Supply voltage, +5 V	7	GND	Ground (Ø V)

Description

The DL 1414 is a four digit display module having 16 bar segments plus a decimal segment and a built-in CMOS integrated circuit.

The IC contains memory, ASCII character generator, and LED multiplexing and drive circuitry. Inputs are TTL compatible. A single 5 V power supply is required. Data entry is asynchronous and random access. A display system can be built using any number of DL 1414s since each character in any DL 1414 can be addressed independently and will continue to display the character last written until it is replaced by another.

Loading data

Loading data into the DL 1414 is straightforward. The desired data code (DØ...D6) and digit address (AØ, A1) is presented in parallel and held stable during a write cycle. Data entry may be asynchronous and in random order. (Digit Ø is defined as right-hand digit with A1 = AØ = Ø = low).

System interconnection is also straightforward. The least significant two address bits (AØ, A1) are normally connected to the like named inputs of all DL1414s in the system. Data lines are connected to all DL1414s directly and in parallel. Multiple DL1414 systems usually use an external one-of-N decoder chip. The "write" pulse is connected to the CE of the decoder. A 3-to-8 line decoder multiplexer (74138) or a 4-to-16 line decoder/multiplexer (74154) are possible choices. All higher-order address bits (above A1) become inputs to the decoder.

Optoelectronic characteristics at 25 °C

Maximum ratings

Voltage, any pin with respect to GND	−0.5...+6.0 V
Operating temperature	−20 ...+65 °C
Storage temperature	−20 ...+70 °C
Relative humidity at 65 °C (non-condensing)	85 %

Optical characteristics (typical)

Luminous intensity per digit/8 segments at 5 V	0.5 mcd
Viewing angle[1])	±40 degrees
Spectral peak wavelength	660 nm
Digit size	2.85 mm

DC characteristics

Symbol	Parameter	−20 °C typ.	+25 °C[3])	+65 °C typ.	Test conditions
I_{CC}	V_{CC} supply current (10 segs/digit)	100 mA	90 mA max.	70 mA	V_{CC} = 5.0 V
I_{CC}	V_{CC} supply current (display blank)		2.7 mA max.		V_{IN} = 0 V V_{CC} = 5.0 V $\overline{WR}$ = 5.0 V
I_{IL}	Input current – low	180 µA	160 µA max.	100 µA	V_{IN} = 0.8 V V_{CC} = 5.0 V
V_{IL}	Input voltage – low		0.8 V max.		V_{CC} = 4.5 V
V_{IH}[2])	Input voltage – high		2.7 V min.		V_{CC} = 4.5 V
			3.3 V min.		V_{CC} = 5.5 V

[1]) "Off Axis Viewing Angle" is here defined as: "the minimum angle in any direction from the normal to the display surface at which any part of any segment in the display is not visible".

[2]) $V_{CC} \geqq V_{IH} \geqq 0.6 \cdot V_{CC}$.

[3]) V_{CC} = +5.0 V ±10 %.

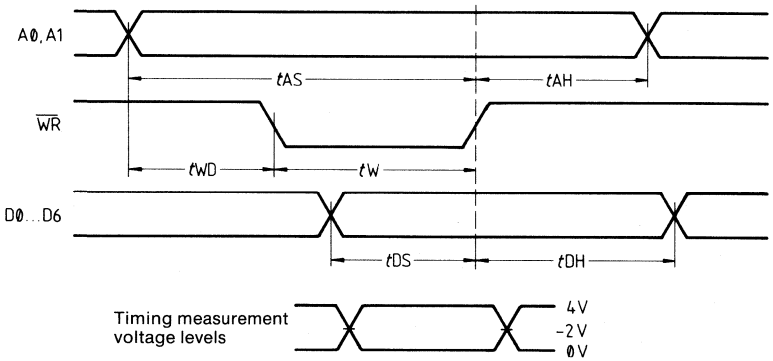
AC characteristics

Minimum timing parameters at V_{CC} = 4.5 V (nanoseconds)

Symbol	Parameter	−20 °C typ.	+25 °C min.	+65 °C typ.
*t*AS	Address setup	300	400	500
*t*WD	Write delay	50	75	125
*t*W	Write pulse	250	325	375
*t*DS	Data setup	200	250	300
*t*DH	Data hold	50	50	100
*t*AH	Address hold	50	50	100

Timing characteristics

Write cycle waveforms



Notes

1) This display contains a CMOS integrated circuit. Normal CMOS handling precautions should be taken to avoid damage due to high static voltages or electric fields.
2) Unused inputs must be tied to an appropriate logic voltage level (either V+ or V−).
3) **Warning** – Do not use solvents containing alcohol.

Character set

				DØ	L	H	L	H	L	H	L	H
				D1	L	L	H	H	L	L	H	H
				D2	L	L	L	L	H	H	H	H
D6	D5	D4	D3									
L	H	L	L		!	"	#	$	%	&	'	
L	H	L	H	(	)	*	+	,	-	.	/	
L	H	H	L	0	1	2	3	4	5	6	7	
L	H	H	H	8	9	:	;	<	=	>	?	
H	L	L	L	@	A	B	C	D	E	F	G	
H	L	L	H	H	I	J	K	L	M	N	O	
H	L	H	L	P	Q	R	S	T	U	V	W	
H	L	H	H	X	Y	Z	[	\	]	^	_	

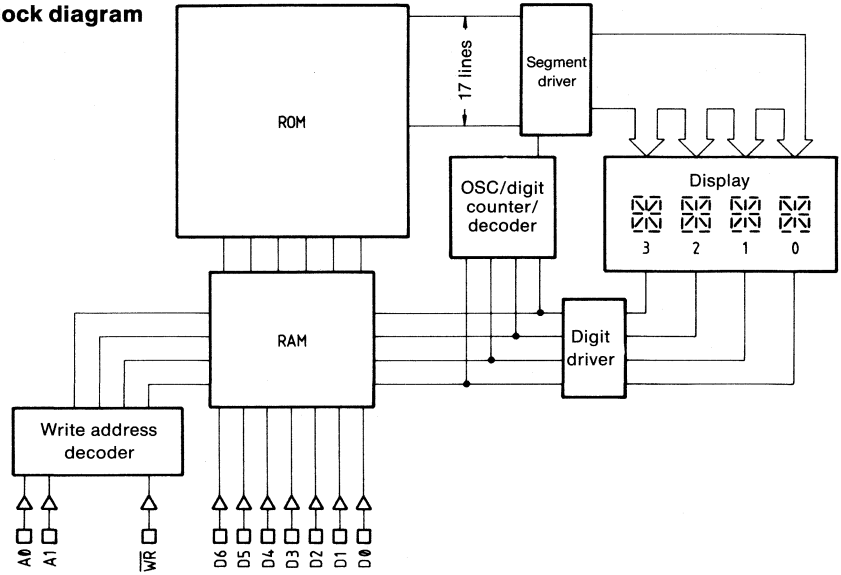
All other input codes display "Blank".

Loading data state table

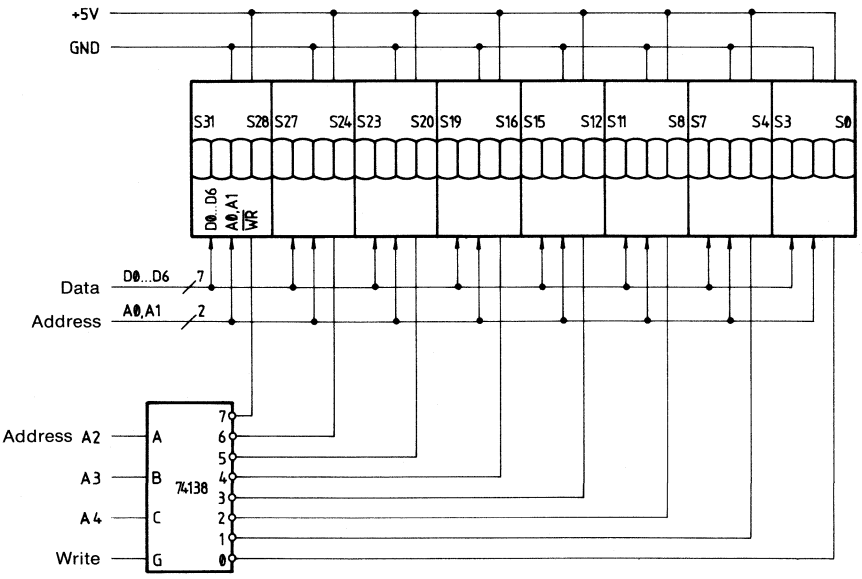
$\overline{WR}$	Address A1	Address AØ	Data input D6	D5	D4	D3	D2	D1	DØ	Digit 3	2	1	Ø
H		Previously loaded display								G	R	E	Y
L	L	L	H	L	L	L	H	L	H	G	R	E	E
L	L	H	H	L	H	L	H	L	H	G	R	U	E
L	H	L	H	L	L	H	H	L	L	G	L	U	E
L	H	H	H	L	L	L	L	H	L	B	L	U	E
L	L	H	H	L	L	L	H	L	H	B	L	E	E
L	L	L	H	L	H	L	H	H	H	B	L	E	W
L	X	X	See character code							See character set			

X = don't care

Block diagram



Typical interconnection for 32 digits



Application Notes Intelligent Display DL1414 with Microprocessors

This application note is intended to serve as a design and application guide for users of the DL1414 alphanumeric intelligent display.

The information presented covers:
device electrical description and operation,
considerations for general circuit design,
and interfacing the DL1414 to microprocessors.

Electrical and mechanical description

General

The internal electronics in the DL 1414 intelligent display eliminates all the traditional difficulties of using multi-digit light emitting displays (segment decoding, drivers, and multiplexing). The intelligent display also provides internal memory for the four digits. This approach allows the user to asynchronously address one of four digits, and load new data without regard to the LED multiplex timing.

Figure 1 is a block diagram of the DL1414. The unit consists of four 17 segment monolithic LED die and a single CMOS integrated circuit chip. The LED die are magnified to a height of 2.8 mm by the built-in lenses. The IC chip contains 17 segment drivers, four digit drivers, 64 character ROM, four word × 7 bit Random Access Memory, oscillator for multiplexing, multiplex counter/decoder, address decoder, and miscellaneous control logic.

Packaging

Packaging consists of an injection-molded plastic lens which also serves as an "encapsulation shell" since it covers five of the six "faces". The assembled and tested substrate (ceramic or "PTF" multilayer) is placed within the shell and the entire assembly is then filled with a water-clear IC-grade epoxy.

This yields a very rugged part which is quite impervious to moisture, shock, and vibration. Although not "hermetic", the device will easily withstand total immersion in water/detergent solutions.

Figure 1
Block diagram

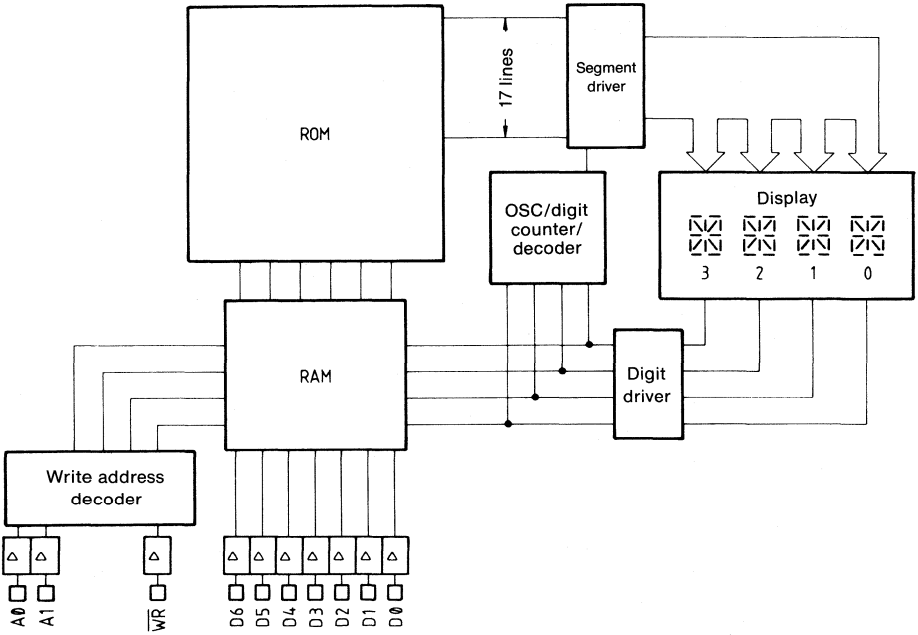
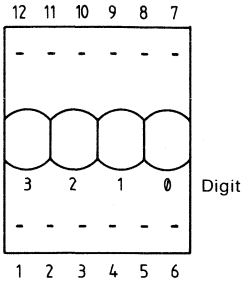


Figure 2
Pin configuration (top view – display side)



Pin	Function		Pin	Function	
1	D5	Data input	12	D6	Data input (MSB)
2	D4	Data input	11	D3	Data input
3	$\overline{WR}$	Write	10	D2	Data input
4	A1	Digit select	9	D1	Data input
5	AØ	Digit select	8	DØ	Data input (LSB)
6	V_{CC}	Supply voltage, +5 V	7	GND	Ground (Ø V)

Electrical inputs

V_{CC} Positive supply +5 V

GND Ground

DØ...D6 Data lines
The seven data input lines are designed to accept the first 64 ASCII characters. See **figure 3** for character set. (The DL1414 interprets all undefined codes as a blank).

AØ, A1 Address lines
The address determines the digit position to which the data will be written. Address order is right to left for positive-true logic.

$\overline{WR}$ Write (active low)
Data and address to be loaded must be present and stable before and after the trailing edge of write (see data sheet for timing info).

Figure 3
Character set

		D0	L	H	L	H	L	H	L	H
		D1	L	L	H	H	L	L	H	H
		D2	L	L	L	L	H	H	H	H
D6	D5	D4	D3							
L	H	L	L		!	"	#	$	%	&	'
L	H	L	H	(	)	*	+	,	-	.	/
L	H	H	L	0	1	2	3	4	5	6	7
L	H	H	H	8	9	:	;	<	=	>	?
H	L	L	L	@	A	B	C	D	E	F	G
H	L	L	H	H	I	J	K	L	M	N	O
H	L	H	L	P	Q	R	S	T	U	V	W
H	L	H	H	X	Y	Z	[	\	]	^	_

All other input codes display "Blank".

Operation

Multiplexed display systems sequentially read and display data from a memory device. In synchronous systems, control circuitry must compare the location of data to be read to the location or position of new data to be stored or displayed, i.e., synchronize before a Write can be done. This can be slow and cumbersome.

Data entry in "intelligent displays" is asynchronous and may be done in any random order. Loading data is similar to writing into a RAM. Each digit has its own memory location and will display until replaced by another code.

The waveforms of **figure 4** demonstrate the relationships of the signals required to generate a Write cycle. (Check individual data sheet for minimum values.) As can be seen from the waveforms, all signals are referenced from the rising or trailing edge of Write.

Figure 4
Timing characteristics (Write cycle waveforms)

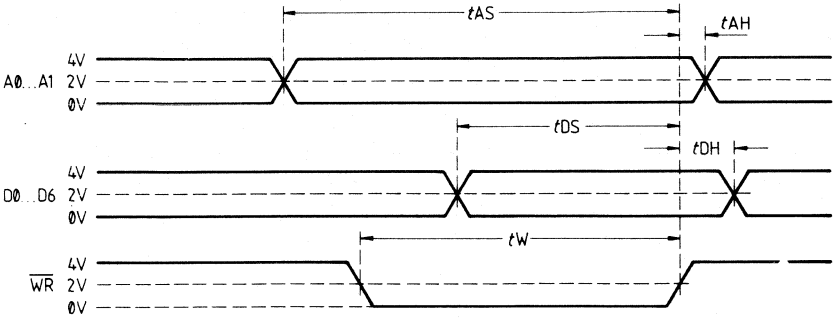


Figure 5
Loading data state table

WR	Address A1	Address AØ	Data input D6	D5	D4	D3	D2	D1	DØ	Digit 3	Digit 2	Digit 1	Digit Ø
H	X	X	X	X	X	X	X	X	X	No change	No change	No change	No change
L	L	L	H	L	L	L	L	L	H	No change	No change	No change	A
L	L	H	H	L	L	L	L	H	L	No change	No change	B	A
L	H	L	H	L	L	L	L	H	H	No change	C	B	A
L	H	H	H	L	L	L	H	L	L	D	C	B	A
L	L	L	H	L	L	L	H	L	H	D	C	B	E
L	H	L	H	L	L	H	L	H	H	D	K	B	E
L	–	–	–	–	–	–	–	–	–	see character set			

X = don't care

General design considerations

Using positive true logic, address order is from right to left. For left to right address order, use the "ones complement" or simple inversion of the addresses.

For systems with only a 6-bit (abbreviated ASCII) code format, data line D6 cannot be left open. Data line D6 must be the complement of data line D5.

When using DL 1414s on a separate display board having more than 15 cm of cable length, it may be necessary to buffer all DL 1414 inputs. This is most easily achieved with Hex non-inverting buffers such as the 74 365 ICs. The object is to prevent transient current in the DL 1414 protection diodes. The buffers should be located on the display board near the DL 1414s.

Local power supply bypass capacitors are also needed in many cases. These should be 6 or 10 V, tantalum type having 10 µF or greater capacitance. Low internal resistance is important due to current steps which result from the internal multiplexing of the DL1414.

If small wire cables are used, it is good engineering practice to calculate the wire resistance of the ground plus the +5 V wires. More than 0.1 V drop, (at 25 mA per digit worst case) should be avoided, since this loss is in addition to any inaccuracies or load regulation limitations of the power supply.

The 5 V power supply for the DL1414s should be the same one supplying V_{CC} to all logic devices which drive the display devices. If a separate supply must be used, then local buffers using hex, non-inverting gates should be used on all DL 1414 inputs and these buffers should be powered from the display power supply. This precaution is to avoid logic inputs higher than display V_{CC} during power up or line transients.

Interfacing the DL1414

A general and straightforward interface circuit is shown in **figure 6**. This scheme can easily interface to µP systems or any other systems which can provide the seven data lines, appropriate address, and control lines.

The DL1414 does not have a chip enable input. Therefore, each DL1414 in a system requires its write pulse be gated with appropriate address signals.

Figure 6
General interface circuit

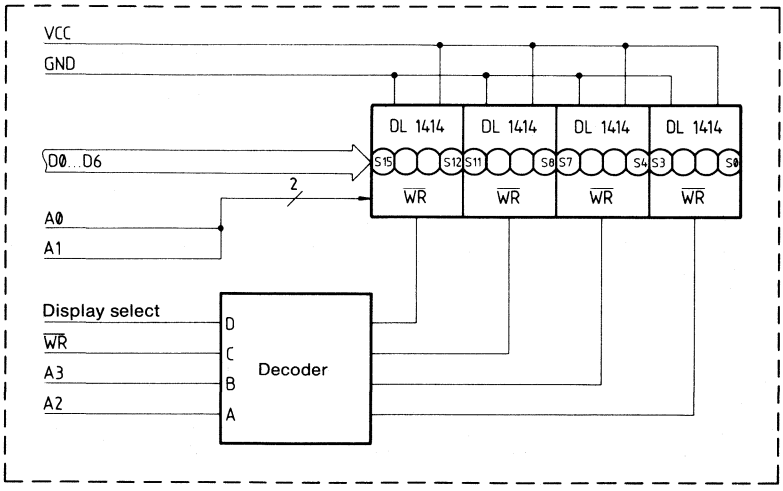


Figure 7
Gating the write pulse

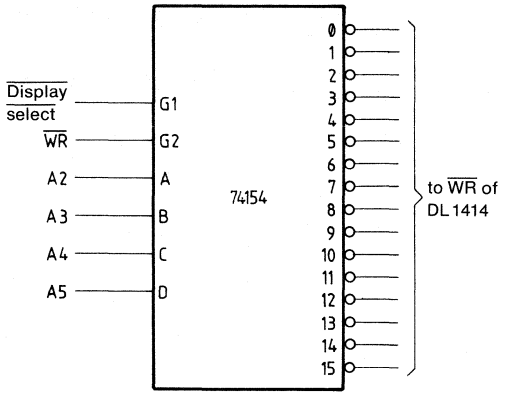


Figure 7a

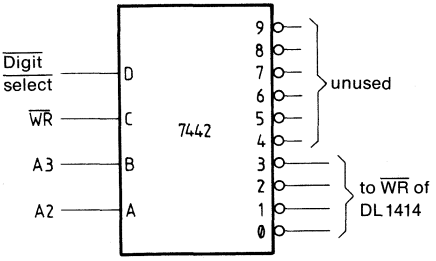


Figure 7b

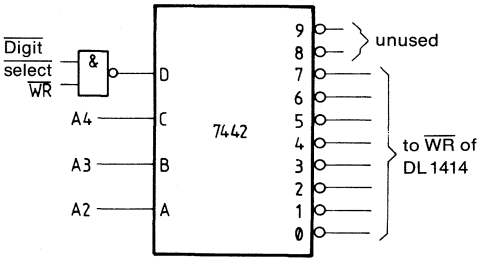


Figure 7c

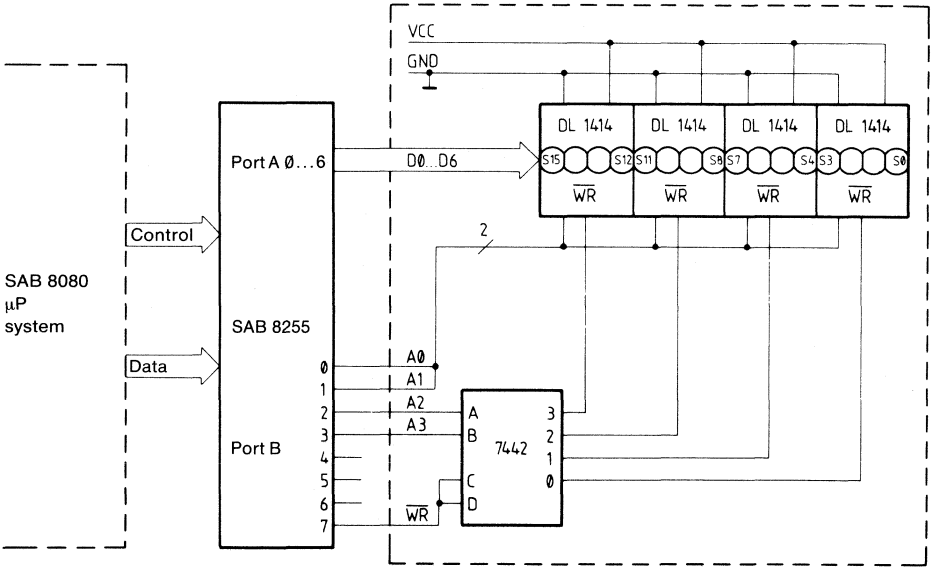
Fig. 7a shows the use of a 74154 decoder (4 line to 16 line) for up to a 64 character display. Using the G1 input for display select (address select in a memory-mapped system) and the G2 input to gate the write signal. Another approach (**figure 7b** and **7c**) which minimizes logic for a 16 or 32 digit display takes advantage of decoding scheme of the 7442 decoder.

Parallel I/O

The parallel I/O device of a microprocessor can easily be connected to the circuit in **figure 6**. One eight bit output port can provide the seven input data bits. Another eight bit output port can contain the address and control signals.

Figure 8 illustrates a 16-character display with an 8080 system using the SAB 8255 programmable peripheral interface I/O device. The following program will display a simple 16-character message using this interface.

Figure 8
16-digit-parallel I/O system



Sample I/O program

```
INIT:   MVI   A, 8ØH    ; Control data mode Ø
        OUT   CONTROL   ; Load control register
        MVI   B, ØØH    ; Set counter = Ø
DISP:   LXI   H, TABLE  ; Set table address
DISP1:  MOV   A, M      ; Move table data to accumulator
        OUT   PORTA     ; Load data port
        MOV   A, B      ;
        CALL  DSPWT     ; Load address and control
        INX   H         ; Increment table address
        INR   B         ; Increment counter
        MVI   A,1ØH     ; Set # of digits
        CMP   B         ;
        JNZ   DISP1     ; 16 characters?
        HALT            ; End of program
DSPWT:  ORI   FØH       ; Set control bits off
        OUT   PORTB     ; Load control
        ANI   7FH       ; Set write bit on
        OUT   PORTB     ; Load write
        ORI   FØH       ; Set write bit off
        OUT   PORTB     ; Load control
        RET             ;
TABLE:  DL              ; ØC3H
        DB              ; ØC9H
        DB              ; ØD4H
        DB              ; ØD3H
        DB              ; ØC1H
        DB              ; ØD4H
        DB              ; ØCEH
        DB              ; ØC1H
        DB              ; ØC6H
        DB              ; ØA0H
        DB              ; ØD3H
        DB              ; ØD4H
        DB              ; ØC8H
        DB              ; ØC7H
        DB              ; ØC9H
        DB              ; ØCCH
```

I/O or memory-mapped addressing

Some designers may wish to avoid the additional cost of a parallel I/O in their system. Structuring the addressing architecture for the DL 1414 to look like a set of peripheral or output devices

(I/O-mapped)

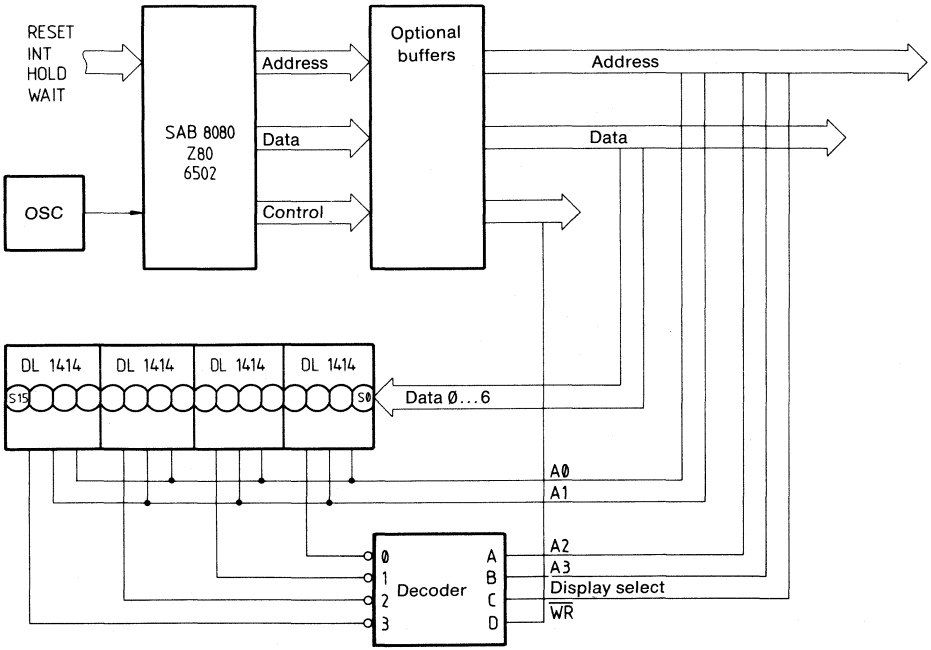
or RAMs and ROMs

(memory-mapped)

is very easy.

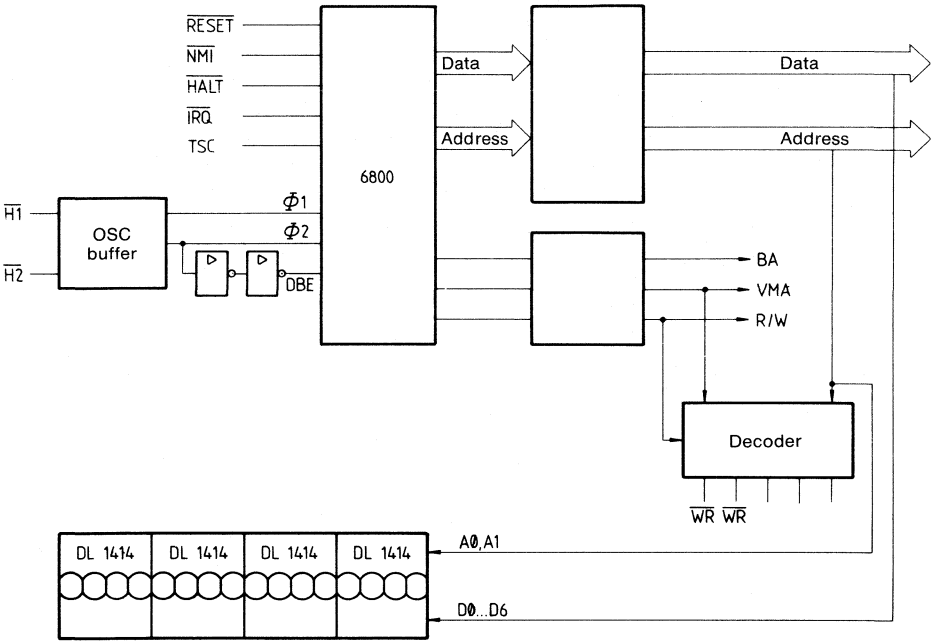
Figure 9 shows the simplicity of interfacing with microprocessors, such as SAB 8080, Z80, and 6502 as examples.

Figure 9
Mapped interface of a 16-digit display to the bus system



The interface with the 6800 microprocessor in **figure 10** illustrates the need for designers to check the timing requirements of the DL 1414 and the μP. The typical data output hold time is only 30 ns for DBE = $\Phi 2$ timing; two inverters in the DBE line are added to increase the data output hold time for compatibility with the 50 ns minimum spec of the DL 1414.

Figure 10
Mapped interface with the 6800 microprocessor



The interface schemes shown demonstrate the simplicity of using the DL1414 with microprocessors. The slight differences encountered with different microprocessors to interface with the DL1414 are similar to those encountered when using different RAMs.

The techniques used in the examples were shown for their generality. The user will undoubtedly invent other schemes to optimize his particular system to its requirements.

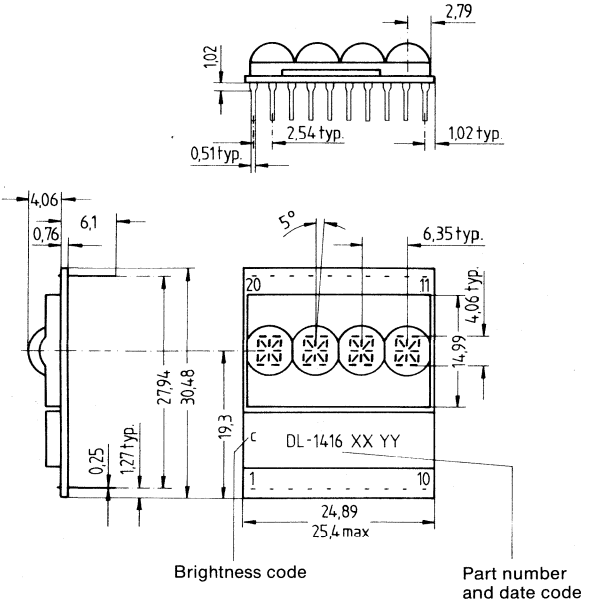
Note that although other manufacturer's products are used in examples, this application note does not imply specific endorsement, or recommendation or warranty of other manufacturer's products by Siemens.

Alphanumeric intelligent display with memory, decoder, and driver.
4.1 mm, red, 4 digits, 16 segments.

Features

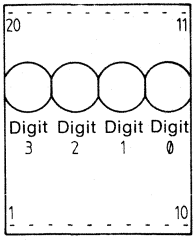
- End-stackable, 4-character package
- High contrast, 4.1 mm high, magnified monolithic characters
- 64-character ASCII format
- Built-in memory, decoder, multiplexer, and drivers
- Direct access to each digit independently and asynchronously
- 5 V logic, TTL compatible
- 5 V power supply only
- Independent cursor function
- Intensity coded for display uniformity

Type	Ordering code
DL 1416	Q68000-A4825-F114



Tolerance ±0.25 mm,
unless otherwise noted

Dimensions in mm



Pin configuration (top view – display side)

Pin	Function	Pin	Function
1	D5 Data input	20	D6 Data input
2	D4 Data input	19	V–
3	DØ Data input	18	V+
4	D1 Data input	17	Unused
5	D2 Data input	16	Unused
6	D3 Data input	15	Unused
7	$\overline{CE}$ Chip enable	14	Unused
8	$\overline{WR}$ Write	13	Unused
9	$\overline{CU}$ Cursor input	12	Unused
10	AØ Digit select	11	A1 Digit select

Description

The DL1416 intelligent display is a four-digit LED display module having a 16-segment font and an on-board CMOS integrated circuit driver.

The CMOS chip includes memory for four digits and cursor, 64 ASCII character generator ROM, and segment/digit drivers with associated multiplexing circuitry. Inputs are TTL compatible as is the power supply requirement. Data entry is asynchronous and random access. A display system can be built using any number of DL1416s since each digit of each DL1416 can be addressed independently. Each digit will continue to display the character last "written" until replaced by another.

A cursor is defined as all segments of a digit position to be lit. The cursor is **not** a character, however, and upon removal leaves the previously displayed character unchanged. Normally, the cursor would be loaded and unloaded (flash) under software control. This can be used as a pointer in a line of DL1416 displays or a "lamp test" function is realized by simply storing a cursor in all four digit positions of a display.

System interconnection is very straightforward. The least significant two address bits (AØ, A1) are connected to the like inputs of all DL 1416s in a system. In small systems having 16 digits (4 DL1416s), the enable ($\overline{CE}$) inputs of the four devices could simply be used directly to select each DL1416. In larger displays, the $\overline{CE}$ inputs would come from A1-of-N decoder IC. In this case, address lines A2...An would go to the decoder inputs. Data lines (DØ...D6) would be connected to all DL1416s directly and in parallel. The cursor ($\overline{CU}$) and write ($\overline{WR}$) lines would also be connected directly and in parallel. The display will then behave as a "write-only memory".

Optoelectronic characteristics at 25 °C

Maximum ratings

Voltage, any pin with respect to GND	$-0.5 \ldots V_{CC} + 0.5$ V
Operating temperature	−20 ... +65 °C
Storage temperature	−20 ... +70 °C
Relative humidity at 65 °C (non-condensing)	85 %

Optical characteristics (typical)

Luminous intensity per digit/8 segments at 5 V	0.5 mcd
Viewing angle	±20 degrees
Spectral peak wavelength	660 nm
Digit size	4.06 mm

DC characteristics

Symbol	Parameter	−20 °C typ.	+25 °C[4])	+65 °C typ.	Test conditions
I_{CC}	V_{CC} supply current (10 segs/char., 4 digits on)		75 mA max.[1])		V_{CC} = 5.0 V
I_{CC}	V_{CC} supply current cursor[2])		100 mA max.[1])		V_{CC} = 5.0 V
I_{CC}	V_{CC} supply current (blank)	5 mA	5 mA max.	2.0 mA	V_{IN} = 0 V V_{CC} = 5.0 V $\overline{WR}$ = 5.0 V
I_{IL}	Input current – low	20 µA	160 µA max.	10 µA	V_{IN} = 0.8 V V_{CC} = 5.0 V
V_{IL}	Input voltage – low		0.8 V max.		V_{CC} = 4.5 V
V_{IH}[3])	Input voltage – high		2.7 V min.		V_{CC} = 4.5 V
			3.3 V min.		V_{CC} = 5.5 V

[1]) Measured at 5 seconds.
[2]) 60 s max. duration.
[3]) $V_{CC} \geqq V_{IH} \geqq 0.6 \cdot V_{CC}$.
[4]) V_{CC} = +5.0 V ±10 %.

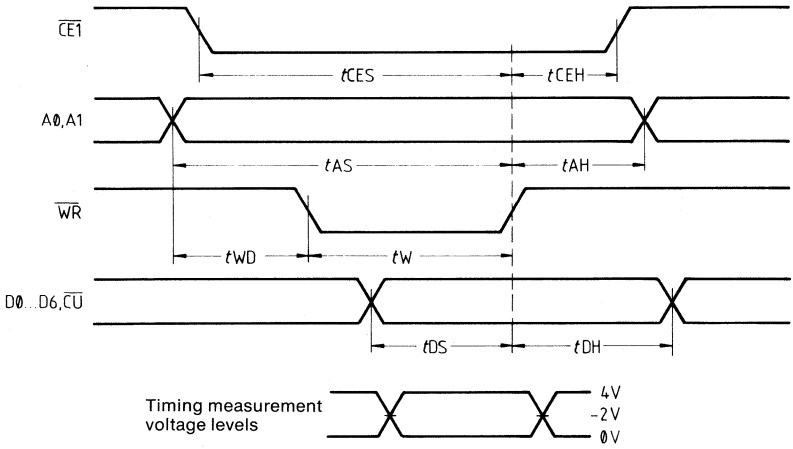
AC characteristics at 25°C

Minimum timing parameters at V_{CC} = 4.5 V (nanoseconds)

Symbol	Parameter	ns
*t*AS	Address setup	1000
*t*WD	Write delay	500
*t*W	Write pulse	500
*t*DS	Data setup	1000
*t*DH	Data hold	400
*t*AH	Address hold	400
*t*CEH	Chip enable hold	400
*t*CES	Chip enable setup	1000

Timing characteristics

Write cycle waveforms



Loading Data

The chip enable ($\overline{CE}$) held low and cursor ($\overline{CU}$) held high will enable data loading. The desired data code (DØ...D6) and selected digit address (AØ, A1) should be held stable while write ($\overline{WR}$) is low for storing new data. The timing parameters in the AC characteristics table are minimum and should be observed. There are no maximum timing requirements. Data entry may be asynchronous and in random order. All undefined data codes (see character set) loaded as data will display a blank.

Digit Ø is defined as the right hand digit with A1 = AØ = Ø = low.

Loading cursor

The chip enable ($\overline{CE}$) and cursor ($\overline{CU}$) are held low. A write ($\overline{WR}$) signal will now load a cursor into any digit position for which the respective first four data lines (DØ, D1, D2, D3) individually or together are held high. If previously stored, the cursors can only be removed if their respective data lines are held low while $\overline{CE}$, $\overline{CU}$ are low and write ($\overline{WR}$) occurs.

The cursor ($\overline{CU}$) should not be hardwired high (off). During the power-up of DL1416s the cursor memory will be in a random state. Therefore, it is recommended for the processor-based system to initialize or write out possible cursors during the system initializing portion of the software.

The cursor display will be overridden by a blank from an undefined code in that digit position.

Notes

1) This display contains a CMOS integrated circuit. Normal CMOS handling precautions should be taken to avoid damage due to high static voltages or electric fields.
2) Unused inputs must be tied to an appropriate logic voltage level (either V+ or V−).
3) **Warning** − Do not use solvents containing alcohol.

Loading data state table

$\overline{CE}$	$\overline{CU}$	$\overline{W}$	Address A1	Address AØ	Data input D6	D5	D4	D3	D2	D1	DØ	Digit 3	Digit 2	Digit 1	Digit Ø
H	X	X	X	X	X	X	X	X	X	X	X	No change	No change	No change	No change
L	H	L	L	L	H	L	L	L	L	L	H	No change	No change	No change	A
L	H	L	L	H	H	L	L	L	L	H	L	No change	No change	B	A
L	H	L	H	L	H	L	L	L	L	H	H	No change	C	B	A
L	H	L	H	H	H	L	L	L	H	L	L	D	C	B	A
L	H	L	L	L	H	L	L	L	H	L	H	D	C	B	E
L	H	L	H	L	H	L	L	H	L	H	H	D	K	B	E
L	H	L	–	–	–	–	–	–	–	–	–	see character set			

X = don't care

Loading cursor state table

$\overline{CE}$	$\overline{CU}$	$\overline{W}$	Address A1	Address AØ	Data input D6	D5	D4	D3	D2	D1	DØ	Digit 3	Digit 2	Digit 1	Digit Ø
H	X	X	X	X	X	X	X	X	X	X	X	D	K	B	E
L	L	L	X	X	X	X	X	L	L	L	H	D	K	B	⊠
L	L	L	X	X	X	X	X	L	L	L	L	D	K	B	E
L	L	L	X	X	X	X	X	L	L	H	L	D	K	⊠	E
L	L	L	X	X	X	X	X	L	H	L	L	D	⊠	B	E
L	L	L	X	X	X	X	X	H	L	L	L	⊠	K	B	E
L	L	L	X	X	X	X	X	H	H	H	H	⊠	⊠	⊠	⊠
L	L	L	X	X	X	X	X	L	L	L	L	D	K	B	E

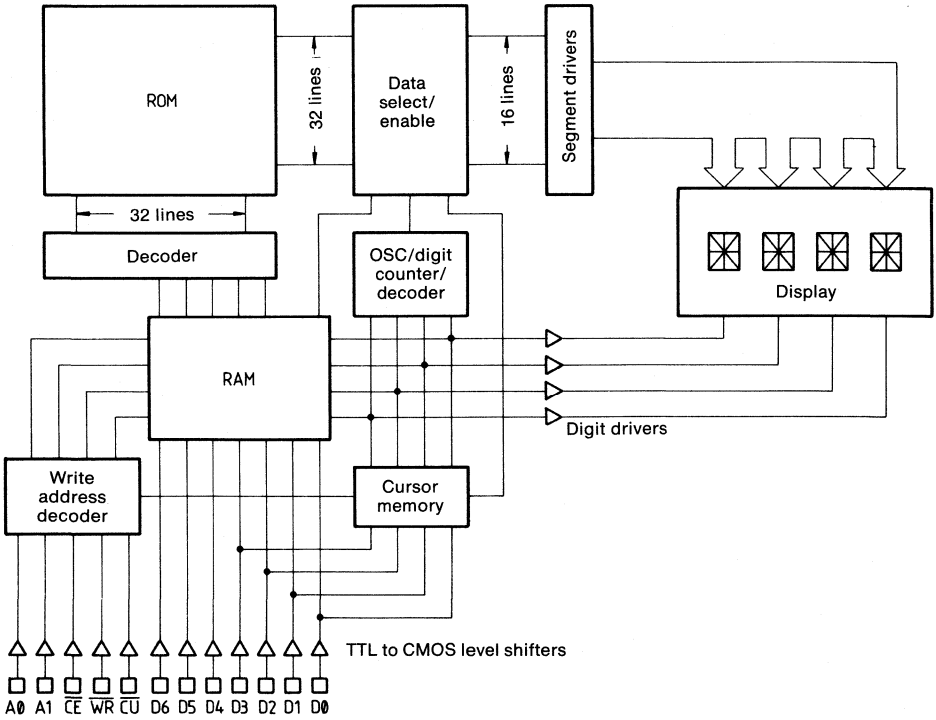
X = don't care

Character set

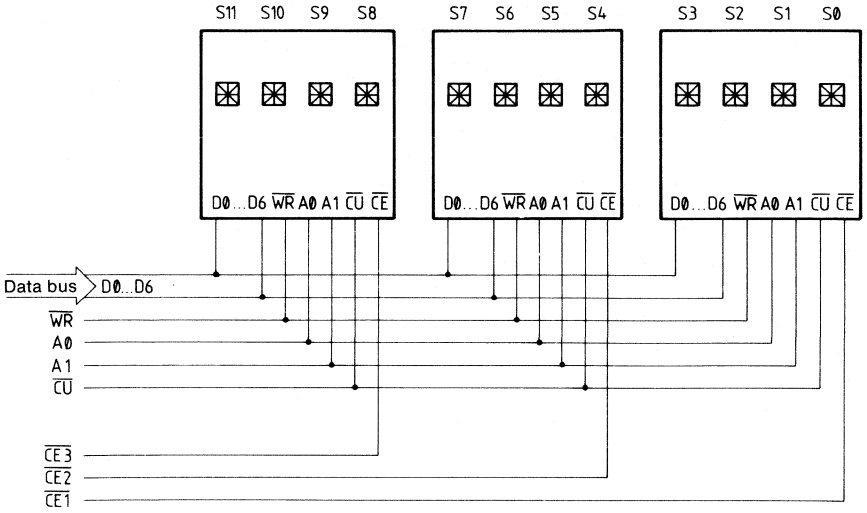
				D0	L	H	L	H	L	H	L	H
				D1	L	L	H	H	L	L	H	H
				D2	L	L	L	L	H	H	H	H
D6	D5	D4	D3									
L	H	L	L									
L	H	L	H									
L	H	H	L									
L	H	H	H									
H	L	L	L									
H	L	L	H									
H	L	H	L									
H	L	H	H									

All undefined data codes that are loaded or occur on power-up will cause à blank display state.

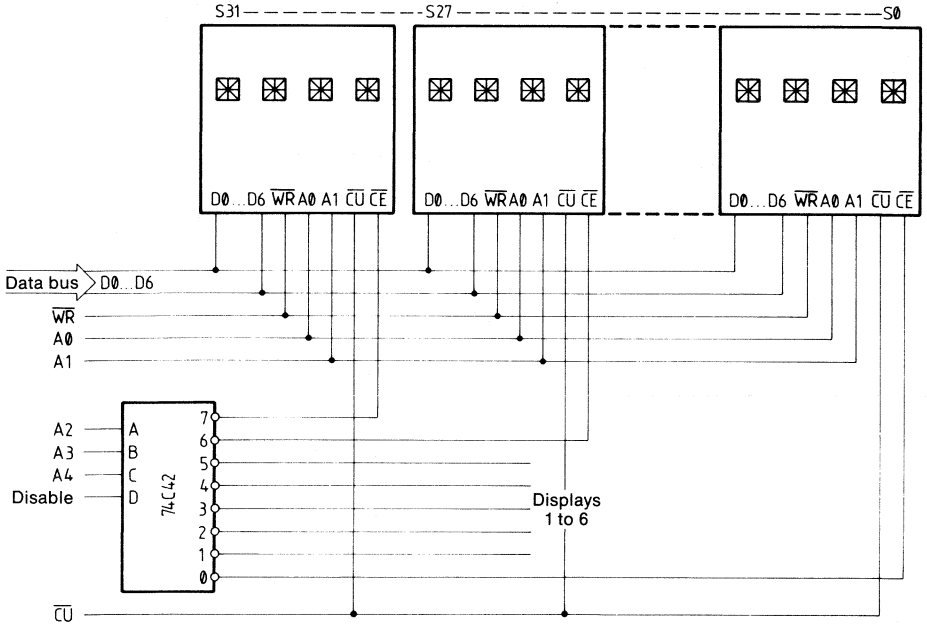
Block diagram



Typical interconnection for small systems, 12 digits



Typical interconnection for 32 digit systems



Application Notes Intelligent Display DL 1416 with and without Microprocessors

1 Display systems with microprocessors

This application note is intended to serve as design and application guide for users of the DL 1416 alphanumeric display.

The information presented covers:
device electrical description and operation,
considerations for general circuit designs,
multi-digit display systems,
interfacing to the 6800, Z80, and SAB 8080 microprocessors.

The DL 1416 was designed to provide an easy-to-use alphanumeric display for the 64 character ASCII systems. Only twelve interconnect pins plus power and ground are needed to drive a single four-digit display. The overall package is designed to allow end-stacking of the DL 1416 to form any desired character length display.

Electrical description

The on-board electronics of the DL 1416 eliminates all the traditional difficulties of using displays – segment decoding, driving, and multiplexing. The DL 1416 has gone further and provided internal memory for the four digits. This approach allows the user to address one of four digits, load the desired data asynchronously to the multiplex rate and continue.

Figure 1 is a block diagram of the circuitry in the DL 1416. The unit consists of a display and a single IC chip. The display is four 16-segment alphanumeric monolithic LED die magnified to a height of 4.1 mm. The IC chip contains the 16 segment drivers, 4 digit drivers, 64-character ROM, four-word 7-bit RAM, internal oscillator for multiplexing, multiplex counter/decoder, cursor RAM, write address decoder, and level shifters for the inputs.

Figure 1
Block diagram

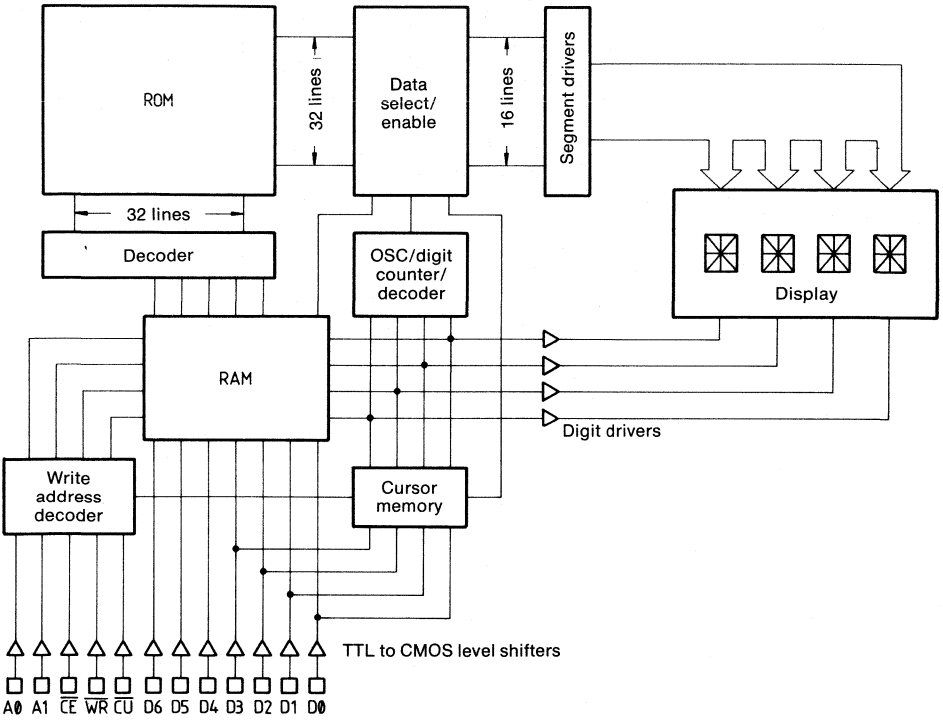
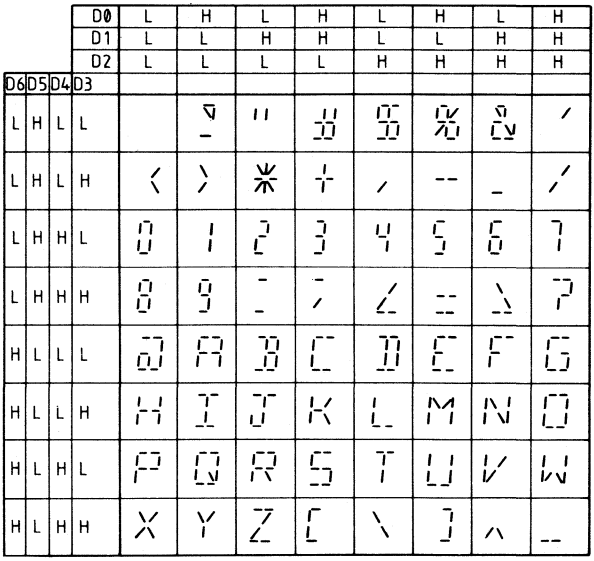


Figure 2
Character set



The inputs to the DL1416 are:

$\overline{CE}$ Chip enable (active low)
This determines which device in an array will actually execute the loading of data. When the chip enable is in the high state, all inputs are inhibited.

AØ, A1 Digit address
The address to the DL1416 determines the digit in which the data will be written. Address order is right-to-left for positive-true address.

DØ...D6 Data lines
The seven data input lines are designed to accept the 64 ASCII code set. See figure 2 for character set.

$\overline{WR}$ Write (active low)
Data to be written into the DL1416 must be present before the leading edge of write. The data and address must be stable until after the trailing edge.

$\overline{CU}$ Cursor (active low)
When the $\overline{CU}$ is held low, the DL1416 enables the user to write or remove a cursor in any digit position. The cursor function lights all 16 segments in the selected digits without erasing the data. After the cursor is removed, the digit will again display the previously written character.

V+ Positive supply
TTL compatible +5 V

V− Negative supply
Ground

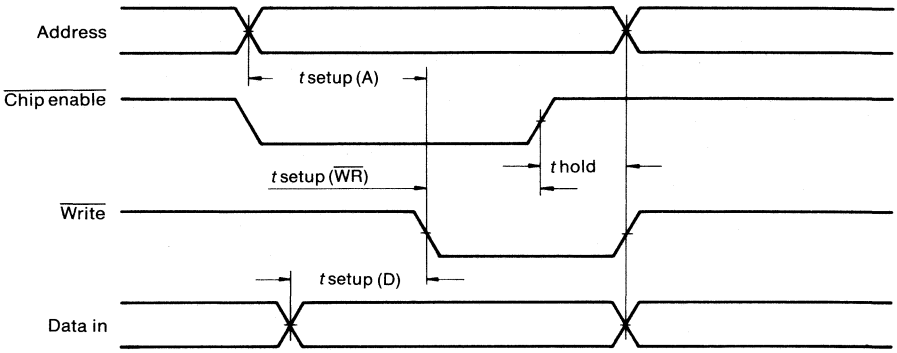
Operation

Loading data into the DL1416 is similar to writing into a RAM. The data and address must be present before the leading edge of the write signal ($\overline{WR}$) and must be present until after the trailing edge. The waveforms of **figure 3** demonstrate the relationship of the signals required to generate a write cycle utilizing chip enable ($\overline{CE}$) and write ($\overline{WR}$) (Check data sheet for minimum values).

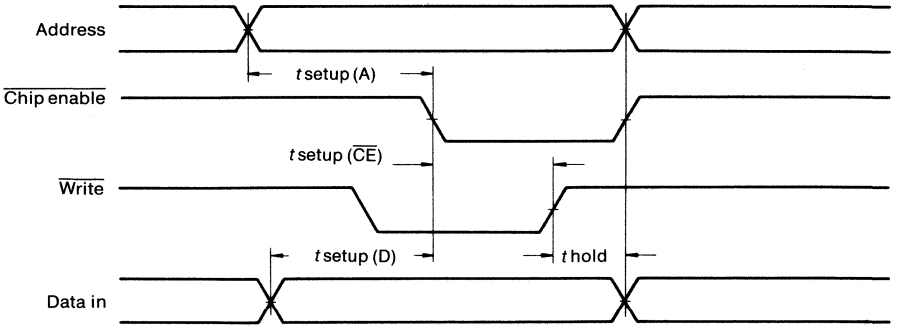
As can be seen from the waveforms, $\overline{CE}$ and $\overline{WR}$ are interchangeable. The true internal "write" function is formed by the "and-of-the-nots".

Multiplexed display systems sequentially read and display data from a memory device. In synchronous systems, control circuitry must compare the location of data to be read and displayed to the location of new data to be stored, i.e. synchronize, before a write can be done. This can be slow if there are many memory locations. It can also be cumbersome.

Figure 3
Write cycle waveforms utilizing Chip Enable ($\overline{CE}$)



Write cycle waveforms utilizing Write ($\overline{WR}$)



Data entry of the DL 1416 is asynchronous and data may be stored in random order. Each digit will continue to display the character last "written" until replaced by another.

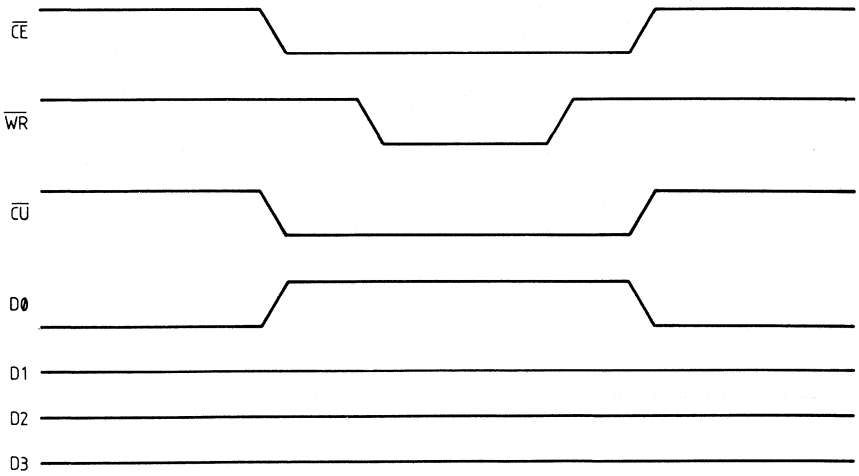
The cursor function causes all 16 segments of a digit to light. The cursor can indicate the position in the display of the next character to be entered. The cursor is not a character but overrides display of the stored character. Upon removal of the cursor, the display will again show the character stored in memory.

The cursor can be written into any digit position by enabling chip enable ($\overline{CE}$), cursor ($\overline{CU}$), the positional data (DØ...D3) and a write ($\overline{WR}$) signal. The position of the cursor will be dependent on which of the first four data lines (DØ, D1, D2, D3) are held high. A high on data line DØ will place a cursor display in the right-most digit and respectively a high on data line D3, will place a cursor display in the left-most digit. The cursor can be loaded into, or erased from more than one position simultaneously by simply holding more than on data line high during the cursor write cycle.

The cursor will remain displayed after the cursor ($\overline{CU}$) and write ($\overline{WR}$) signals have been removed. The waveforms in **figure 3** show a cursor being placed in digit Ø and erased from digit 1, digit 2, and digit 3 simultaneously.

Hardwiring the cursor ($\overline{CU}$) line high is not recommended. This internal cursor memory will be randomly loaded on power-up and all positions must be cleared before a cursor-free display is ensured.

Figure 4
Cursor write cycle



General design considerations

Using positive-true address logic, address order is from right to left. For left to right address order, use the "ones-complement" or simple inversion of the addresses. For systems with only a 6 bit ASCII code format, data line D6 cannot be left open. Data D6 must be the complement of data line D5. If an illegal code is loaded into the DL1416, it will display a blank in the digit accessed.

A "display test" function can be realized by simply storing a cursor in all digits simultaneously. This is done by holding DØ, D1, D2 and D3 high and $\overline{CU}$ low during a cursor write cycle. The same operation, with the data lines low will end "display test".

Because of the random state of the cursor RAM after power up, it is necessary to clear it initially to assure that all the cursors are off.

When using DL 1416s on a separate display board having more than 15 cm of cable length, it may be necessary to buffer all DL1416 inputs. This is most easily achieved with hex-non-inverting buffers such as 74 365 ICs. The object is to prevent transient current in the DL1416 protection diodes. The buffers should be located on the display board near the DL1416s.

Local power supply bypass capacitors are also needed in many cases. These should be 6 or 10 V tantalum type having 10 μF or greater capacitance. Low internal resistance is important to eliminate voltage transients due to the current steps which result from the internal multiplexing of the DL1416.

If small wire cables are used, it is good engineering practice to calculate the wire resistance of the ground plus the +5 V wires. More than 0.1 V drop (at 25 mA per digit worst case) should be avoided, since this loss is in addition to any inaccuracies or load regulation limitations of the power supply.

General interface

The most general and straightforward interface approach would be to use the parallel I/O device of a microprocessor. This interface scheme can be completely software-dependent. One eight bit output port can handle the seven input data bits and the cursor. Another eight bit output port can contain the address and chip enable information with one bit reserved for the write signal.

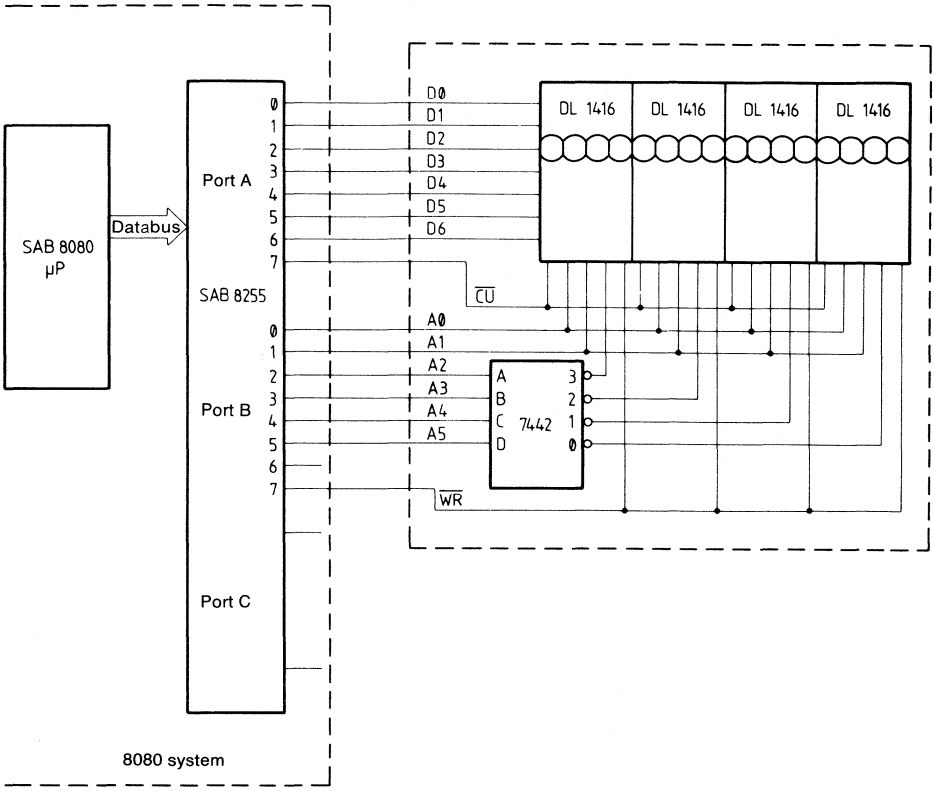
An SAB 8080 system shown in **figure 5** illustrates a 16 character display using an SAB 8255 programmable peripheral interface I/O device with a 7442 one-of-ten decoder added for ease of programming.

The following program will display a simple 16 character message using the parallel I/O interface.

Sample I/O program

```
INIT:   MVI   A, 8ØH    ; Control data mode Ø
        OUT   CONTROL   ; Load control register
CUSR:   MVI   A, ØØH    ; Clear cursor data
        OUT   PORTA     ; Load data port
        MVI   B, OFH    ; Set counter
CUSR1:  MOV   A, B      ;
        CALL  DSPWT     ; Write subroutine
        DCR   B         ; Decrement counter
        JNZ   CUSR1     ; 16 characters
DISP:   LXI   H, TABLE  ; Set table
DISP1:  MOV   A, M      ;
        OUT   PORTA     ; Load data output
        MOV   A, B      ;
        CALL  DSPWT     ; Load address and write
        INX   H         ; Increment table address
        INR   B         ; Increment counter
        MVI   A, 1ØH    ; Set # of digits
        CMP   B         ;
        JNZ   DISP1     ; 16 characters
        HLT             ; End of program
DSPWT:  ORI   8ØH       ; Set write bit off
        OUT   PORTB     ; Load address
        ANI   7FH       ; Set write bit on
        OUT   PORTB     ; Load write
        ORI   8ØH       ; Set write bit off
        OUT   PORTB     ; Load write
        RET             ;
TABLE:  DB              ; ØC3H
        DB              ; ØC9H
        DB              ; ØD4H
        DB              ; ØD3H
        DB              ; ØC1H
        DB              ; ØD4H
        DB              ; ØCEH
        DB              ; ØC1H
        DB              ; ØC6H
        DB              ; ØA0H
        DB              ; ØD3H
        DB              ; ØD4H
        DB              ; ØC8H
        DB              ; ØC7H
        DB              ; ØC9H
        DB              ; ØCCH
```

Figure 5
16-character display using an SAB 8255 parallel I/O device



I/O or memory-mapped addressing

Some designers may wish to avoid the additional cost of a parallel I/O device in their system. Structuring the addressing architecture for the DL1416 to look like a set of peripheral or output devices

(I/O-mapped)

or RAMs and ROMs

(memory-mapped)

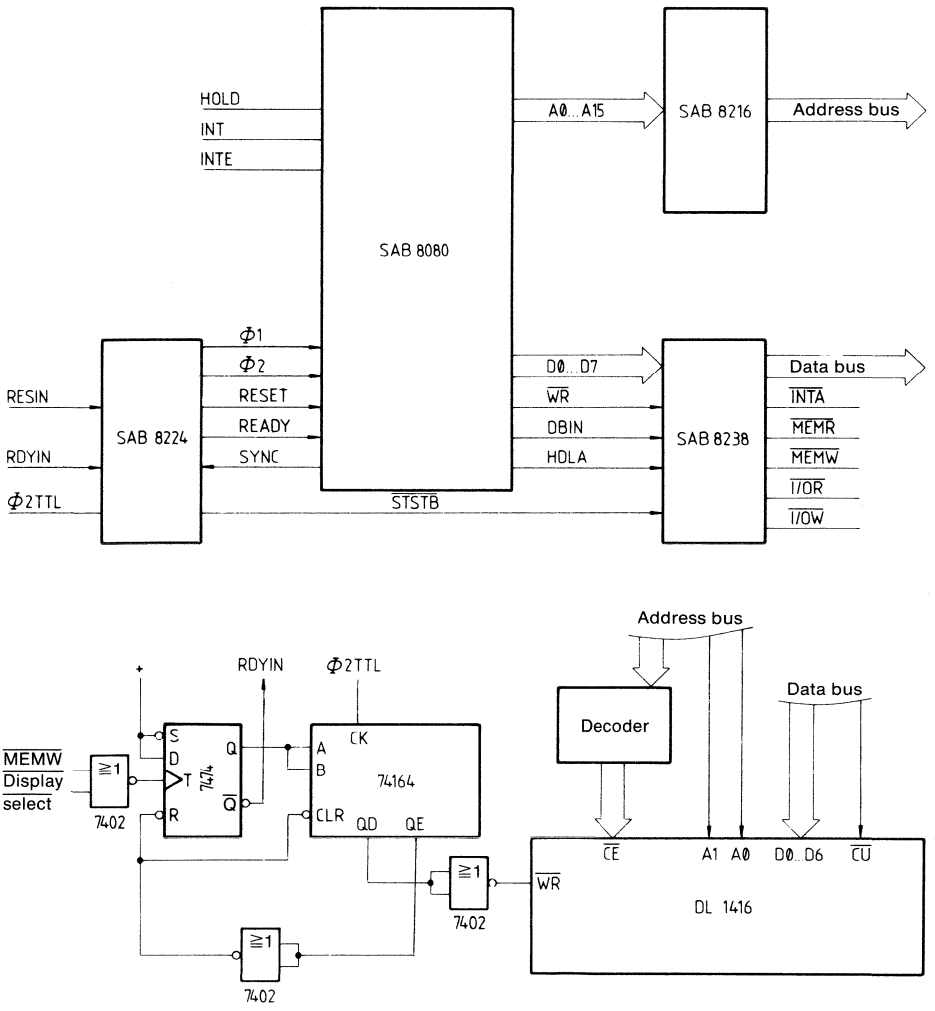
is very easy.

However, the set-up and hold times of the DL1416 are too slow for some present µPs running at maximum speed. To operate at maximum clock rates, the processor must be made to pause for the required display write cycle interval.

DL 1416/8080 interface

Microprocessors like the 8080 and Z80 have the ability to generate "wait states" for use with relatively slow memories. **Figure 6** shows a circuit which utilizes "wait states" to interface the DL 1416 display to an 8080 system with a *t*CY = 500 ns.

Figure 6

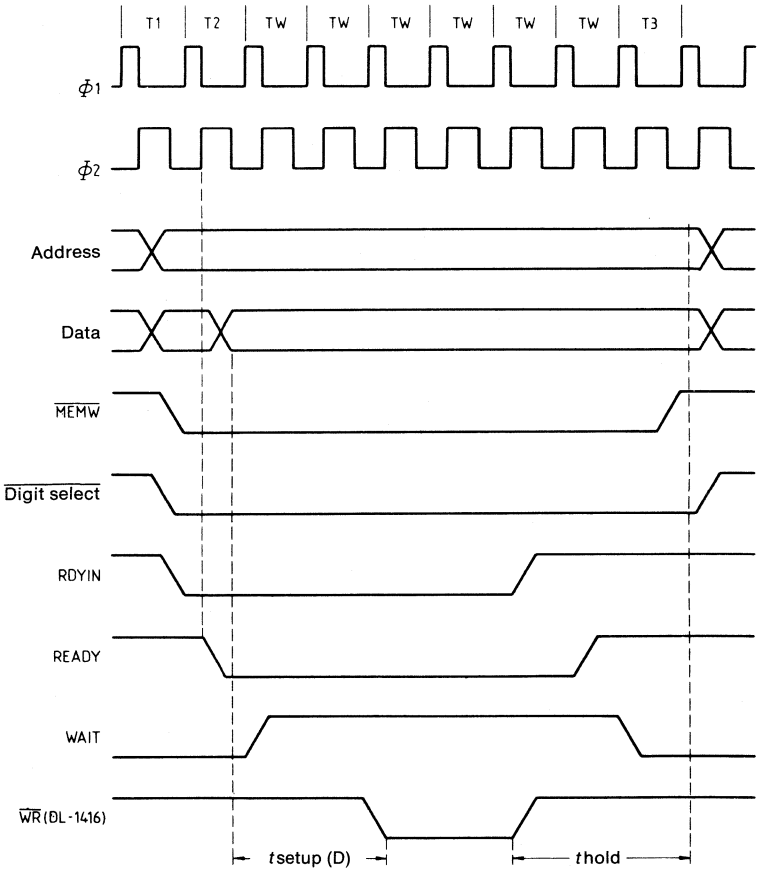


The signal $\overline{\text{MEMW}} \bullet \overline{\text{DISPLAY SELECT}}$ defines a DL 1416 display write cycle and initiates the RDYIN signal. $\overline{\text{MEMW}}$ alone would generate wait states for all write cycles and would slow down total computation. The shift register, 74164, is useful for generating a DL 1416 write signal which meets the setup times for different processor clock rates.

The timing diagram, **figure 7,** illustrates the relationship between write, wait, and DL 1416 write.

Note: System controller SAB 8238 required for an early $\overline{\text{MEMW}}$ signal.

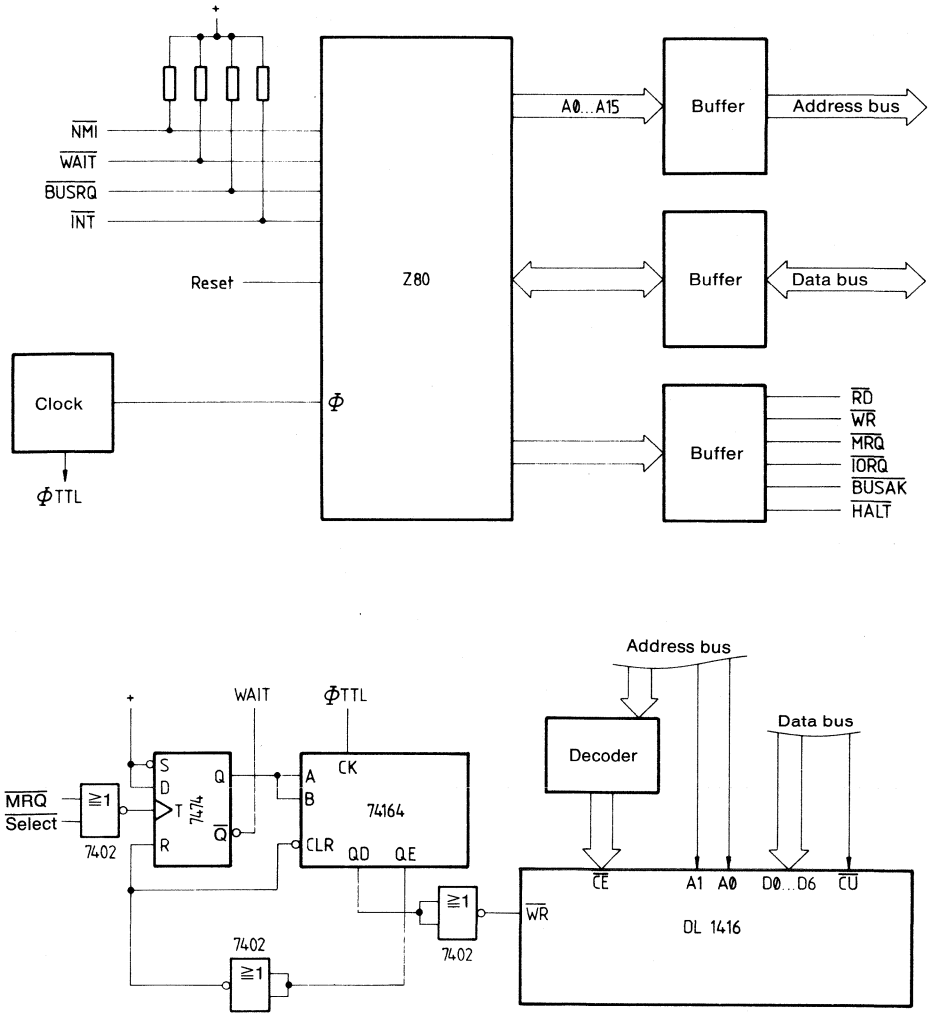
Figure 7



DL 1416/Z80 interface

The organization of the Z80 is very similar to the 8080 processor. Both processors utilize wait states for slow memory and, as can be seen in figure 8, the interface can be identical to the 8080 system. For *t*CY = 500 ns, only the signal names are different.

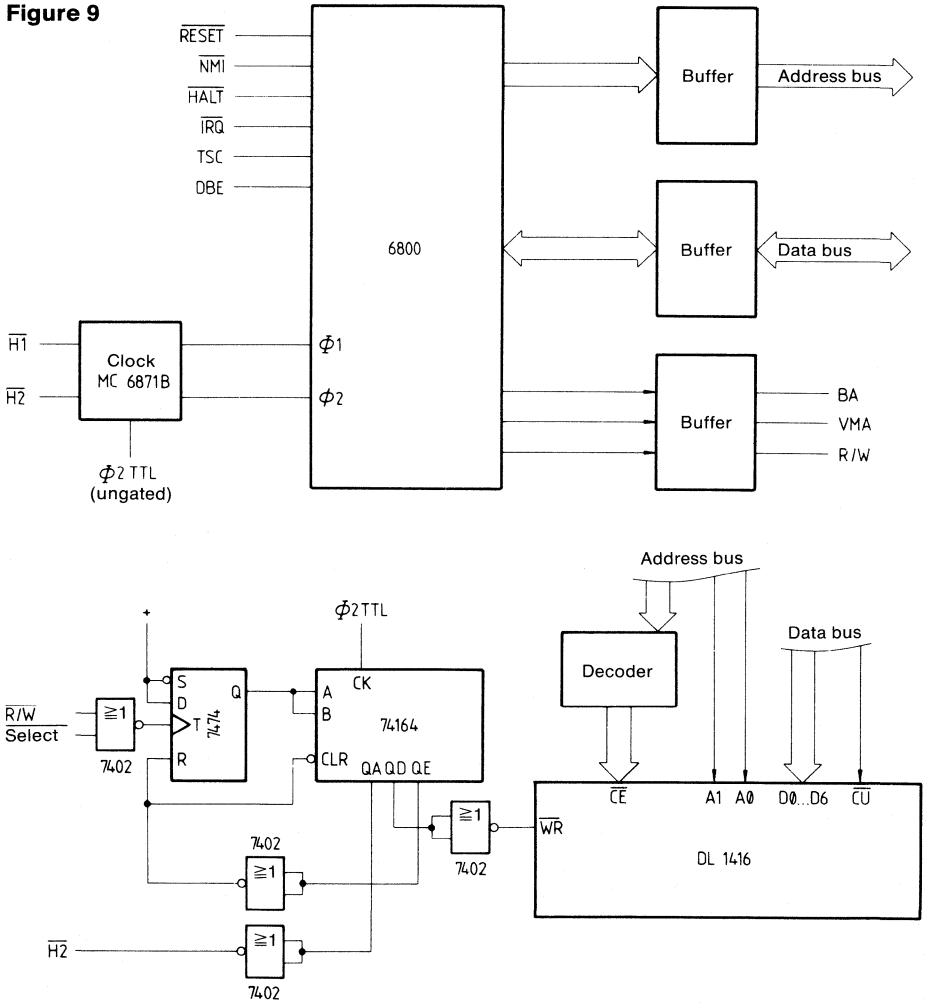
Figure 8



DL 1416/6800 interface

For processors such as the 6800 that do not have wait state capability, clock pulse stretching techniques can be used. Microprocessor clocks such as the Motorola MC6871B have the ability to hold either $\Phi 1$ or $\Phi 2$. **Figure 9** uses the same interface techniques as for the 8080 and Z80. The signal $\overline{H2}$ extends the $\Phi 2$ clock. All address and data lines will remain valid until $\overline{H2}$ is released. $\overline{H2}$ was taken from the output of the first stage of the shift register in this case to synchronize with $\Phi 2$; otherwise a narrow $\Phi 1$ may result.

Figure 9



Conclusion

The interface schemes shown demonstrate the general simplicity of DL1416 use with microprocessors. The differences among the examples are in providing proper write signals. Because of the setup and hold times of the DL1416, many microprocessor systems require some type of interface circuitry for compatibility. The techniques used in these examples were chosen for their versatility in accepting a wide range of clock rates. The user will undoubtedly invent other schemes to optimize his particular system to its requirements.

This **application note** is not intended to imply specific endorsement or warranty of other manufacturer's products by Siemens.

2 Display systems without a microprocessor

The DL 1416, 4 digit 16 segment, alphanumeric "intelligent" display, and succeeding products in the family, have on board memory, decoder, and drive circuitry. This makes it particularly well suited to marry directly to a microprocessor. However, small multi-message systems of 4, 8, 12, 16 character length need not have a microprocessor to drive the alphanumeric display. The DL 1416 with the aid of PROM can combine lighted indicators, status displays, annunciator messages or symbols, or a "canned message" into a single display.

Annunciator displays

An automobile, for example, has several switches each lighting its own status or annunciator indicator. A single DL 1416 alphanumeric display could easily display messages alternately upon interrogation of the appropriate switches.

The circuit shown in **figure 10** will display four character messages sequentially for each open switch and continue to display until switches are returned to their normally closed positions. The counters U4 and U5 address the PROM U6 and select switches on U1. The data selector, U1, sequentially selects one of eight switches (oil, temperature, catalytic, generator, brake, door, belt, and null). The eighth switch or null state can display a blank for a normal or off condition.
The output of U1 enables the DL 1416, $\overline{CE}$. When this signal goes high, the monostable, U2, will fire and inhibit the oscillator U3 for approximately a two-second display time. The PROM, U6, generates the ASCII code data for each word. Expansion of the display can easily be achieved by adding a PROM for each additional DL 1416.

Another annunciator type display is shown in **figure 11**. This display has a message of up to 16 characters and will continue to display the same line until the 6 bit input code changes state. With this scheme, it can be seen that the 16 character X64 line message PROM can easily be adapted for other message and character length combinations.

Figure 10

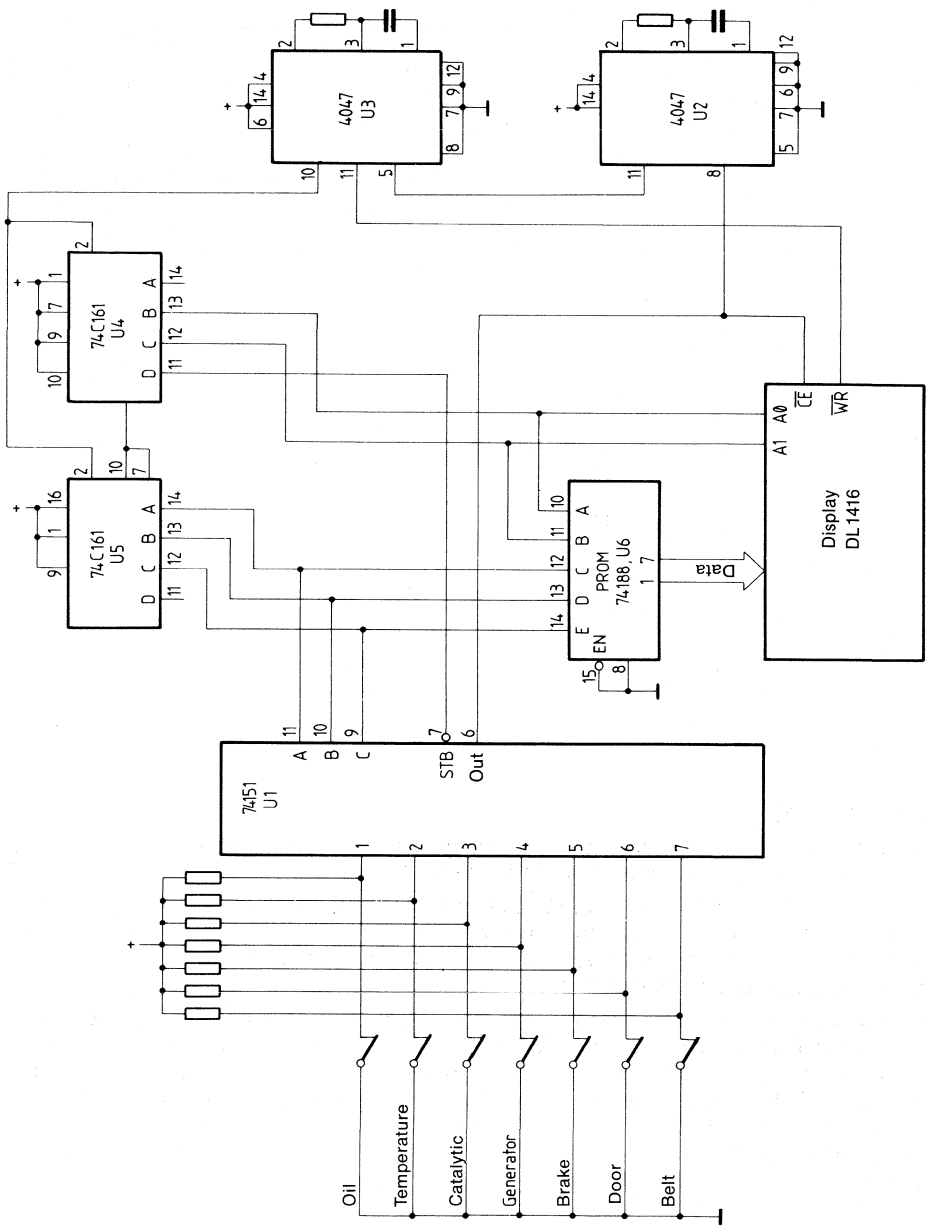
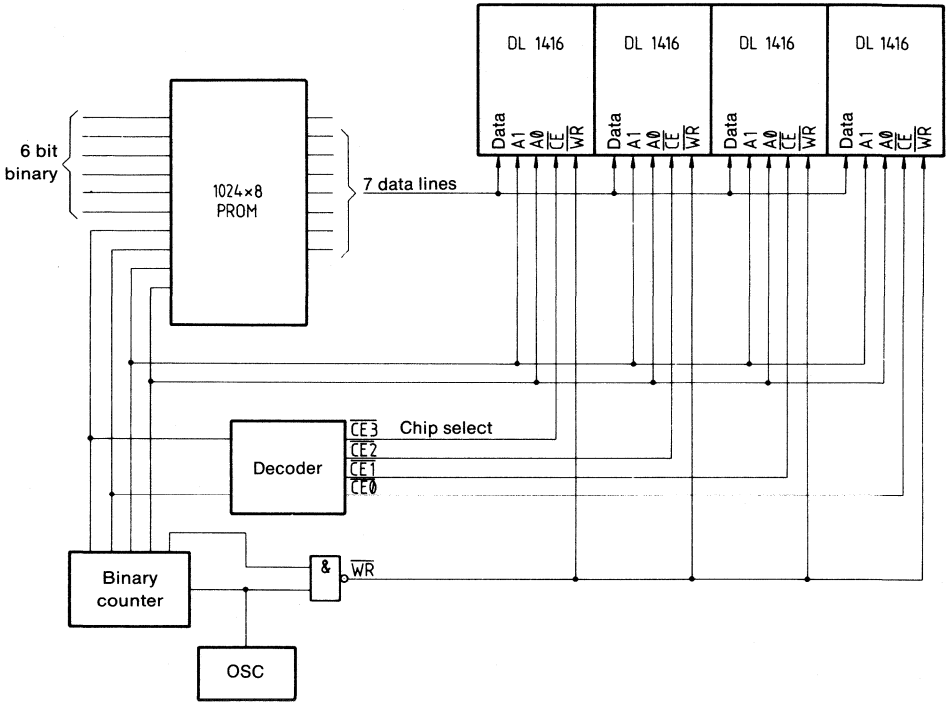

4047
U3
4047
U2
74C161
U4
74C161
U5
PROM
74188, U6
Display
DL1416
Data
74151
U1
STB
Out
Oil
Temperature
Catalytic
Generator
Brake
Door
Belt

Figure 11
Typical circuit for 64 messages, 16 characters long



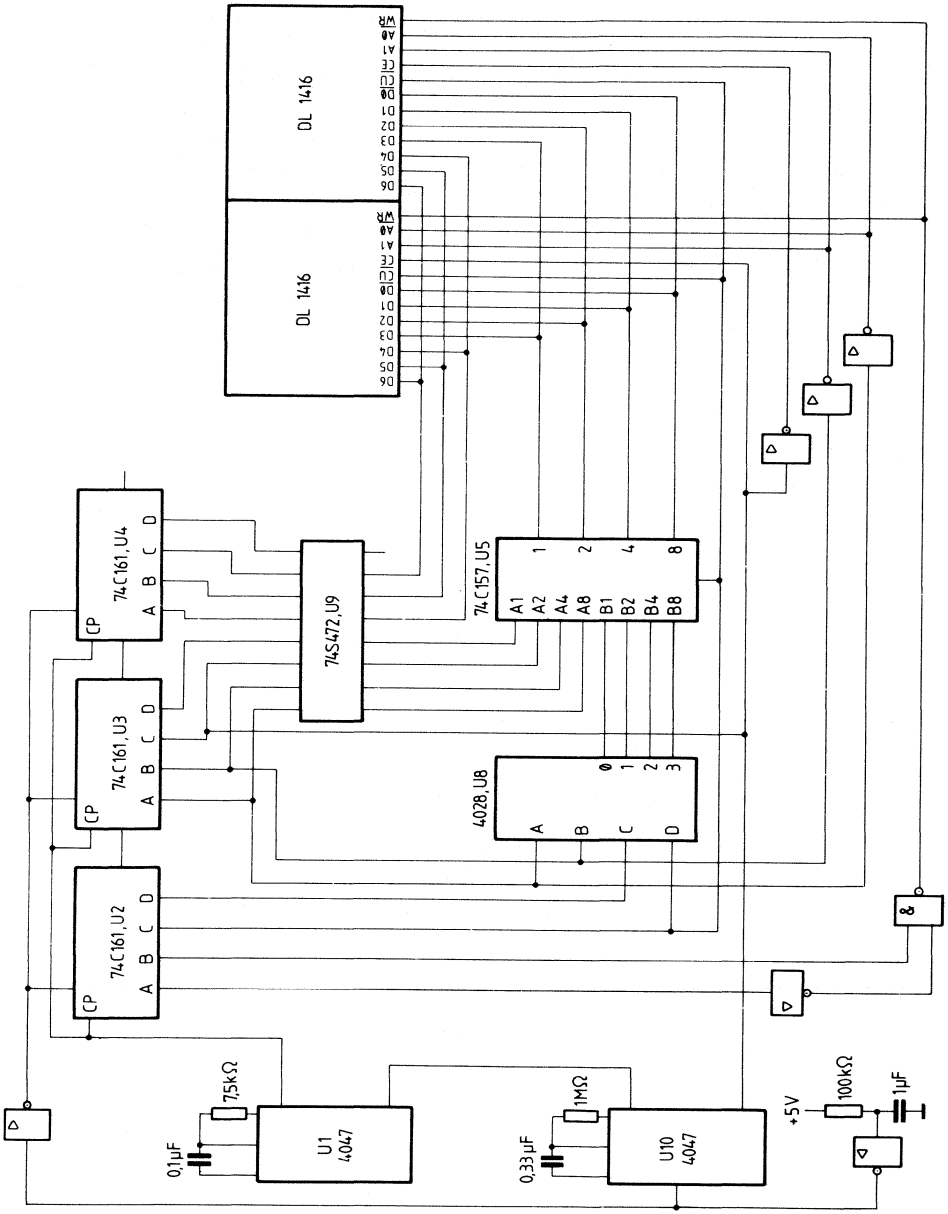
Canned messages

The canned message type display can be an ideal sales, marketing, or instructional aid. The message can be altered by replacing the PROM.

The technique for this display would be to sequentially display a word or group of words, depending on the character length of the display, through the entire message. The system could either continue to repeat itself or could go through the complete sequence once each time a switch is operated.

Figure 12 is the schematic for a sales demo box for the DL1416. A 256×8 PROM was used to display an 8 digit-32 word message. The oscillator, U1, increments the counters U2, U3, U4 providing the address for the DL1416s and PROM U9. After eight counts the monostable U10 is fired, inhibiting the oscillator for a two second display time. Devices U5 and U8 were added for cursor control. Decoder U8 will alternately enable or disable a data bit for a cursor to proceed writing new data into each digit. The multiplexer U5 will select the character data or the cursor data for the DØ...D3 data lines. Inverters on the address lines cause data entry to occur from the left rather than from the right.

Figure 12

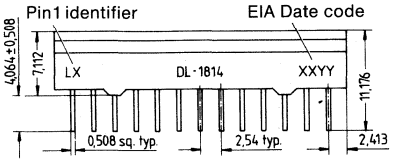

DL 1416
DL 1416
74C161, U4
74C161, U3
74C161, U2
74S472, U9
74C157, U5
4028, U8
7,5kΩ
0,1µF
U1
4047
1MΩ
0,33µF
U10
4047
+5V
100kΩ
1µF

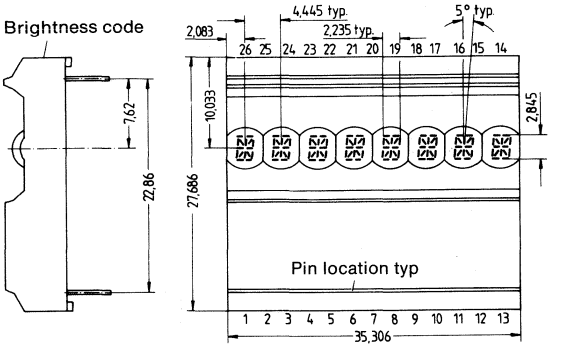
Alphanumeric intelligent display with memory, decoder, and driver.
2.8 mm, red, 8 digits, 17 segments.

Features

- 2.8 mm high, magnified monolithic characters
- Wide viewing angle, ±33 degrees
- Rugged solid plastic encapsulated package
- Fast access time, 500 ns
- Compact size for hand-held equipment
- Fully integrated CMOS IC containing
  - memory
  - character generator
  - multiplex and LED drive circuitry
- Direct access to each digit independently and asynchronously
- TTL compatible, 5 V power supply
- 17th segment for improved punctuation marks
- Low power consumption, typically 10 mA per character
- Display blank function
- Intensity coded for display uniformity
- End-stackable, 8 character package

Type	Ordering code
DL 1814	Q68000-A7156-F114





Dimensions in mm

Tolerance ±0.25 mm,
unless otherwise specified

Pin configuration (top view – display side)

Pin	Function		Pin	Function	
1	DØ	Data input (LSB)	26	$\overline{CE}$	Chip enable
2	D1	Data input	25		No pin
3	D2	Data input	24		No pin
4	D3	Data input	23		No pin
5	D4	Data input	22		No pin
6	D5	Data input	21		No pin
7	D6	Data input (MSB)	20		No pin
8	GND	Ground (Ø V)	19		No pin
9	AØ	Digit select	18		No pin
10	A1	Digit select	17		No pin
11	A2	Digit select	16		No pin
12	$\overline{WR}$	Write	15		No pin
13	V_{CC}	Supply voltage +5 V	14	$\overline{BL}$	Blanking

Description

The DL1814 is an 8 digit display module having 16 bar segments plus a decimal segment and a built-in CMOS integrated circuit.

The IC contains a memory, ASCII character generator and LED multiplexing and drive circuitry. The inputs are TTL compatible. A single 5 V power supply is required. Data entry is asynchronous and random access. A display system can be built using any number of DL1814s since each character in any DL1814 can be addressed independently and will continue to display the character last written until it is replaced by another.

Loading data

Loading data into the DL1814 is straightforward. The desired data (DØ...D6) and chip enable ($\overline{CE}$) should be present and stable during a write pulse ($\overline{WR}$). No synchronization is necessary, and each character will continue to be displayed until it is replaced with another. Multiple displays will require an external decoder IC connected to the chip enable input.

Setting the chip enables $\overline{CE}$ to its true state (i.e. low = Ø V) will enable data loading. The desired data code (DØ...D6) and digit address (AØ, A1, A2) must be held stable during the write cycle for storing new data. Data entry may be asynchronous and random. (Digit Ø is defined as right hand digit with A2 = A1 = AØ = Ø = low.)

Blanking the display

Blanking the display may be accomplished by loading a blank or space into each digit of the display or by using the ($\overline{BL}$) display blank input.

Setting the ($\overline{BL}$) input low does not affect the contents of either data. A flashing display can be realized by pulsing ($\overline{BL}$).

Optoelectronic characteristics at 25 °C

Maximum ratings

Voltage, any pin with respect to GND	−0.5 ... +6.0 V
Operating temperature	−20 ... +65 °C
Storage temperature	−20 ... +70 °C
Relative humidity at 65 °C (non-condensing)	85 %

Optical characteristics (typical)

Luminous intensity per digit/8 segments at 5 V	0.5 mcd
Viewing angle[1])	±33 degrees
Spectral peak wavelength	660 nm
Digit size	2.85 mm

DC characteristics

Symbol	Parameter	min.	typ.	max.	Test conditions
V_{CC}	Supply voltage	4.5 V		5.5 V	
I_{CC}	V_{CC} supply current		2.0 mA	3.7 mA	V_{CC} = 5 V, $\overline{WR}$ = V_{CC}, V_{IN} = Ø, (display blank)
I_{CC}	V_{CC} supply current		80 mA	120 mA	V_{CC} = 5 V, (10 segs/char., 8 digits on)
V_{IL}	Input voltage – low (any input)			1.0 V	V_{CC} = 5 V
V_{IH}*)	Input voltage – high (any input)	3.0 V			V_{CC} = 5 V
I_{IL}	Input current – low (any input)			160 µA	V_{CC} = 5 V, V_{IN} = 0.8 V

*) $V_{CC} \geqq V_{IH} \geqq 0.6\ V_{CC}$

[1]) "Off Axis Viewing Angle" is here defined as: "the minimum angle in any direction from the normal to the display surface at which any part of any segment in the display is not visible".

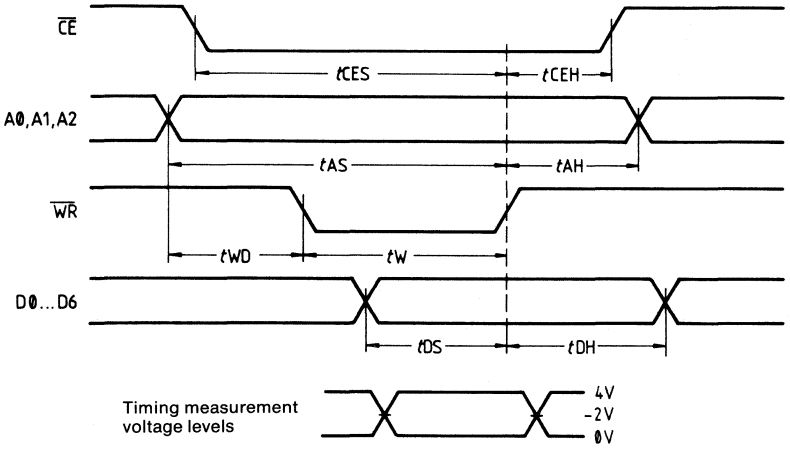
AC characteristics at 25 °C

Minimum timing parameters at V_{CC} = 4.5 V (nanoseconds)

Symbol	Parameter	ns
*t*CES	Chip enable setup	450
*t*AS	Address setup	450
*t*WD	Write delay	150
*t*W	Write pulse	300
*t*DS	Data setup	250
*t*CEH	Chip enable hold	50
*t*AH	Address hold	50
*t*DH	Data hold	50

Timing characteristics

Write cycle waveforms



Notes

1) This display contains a CMOS integrated circuit. Normal CMOS handling precautions should be taken to avoid damage due to high static voltages or electric fields.
2) Unused inputs must be tied to an appropriate logic voltage level (either V+ or V−).
3) **Warning:** Do not use solvents containing alcohol!

Character set

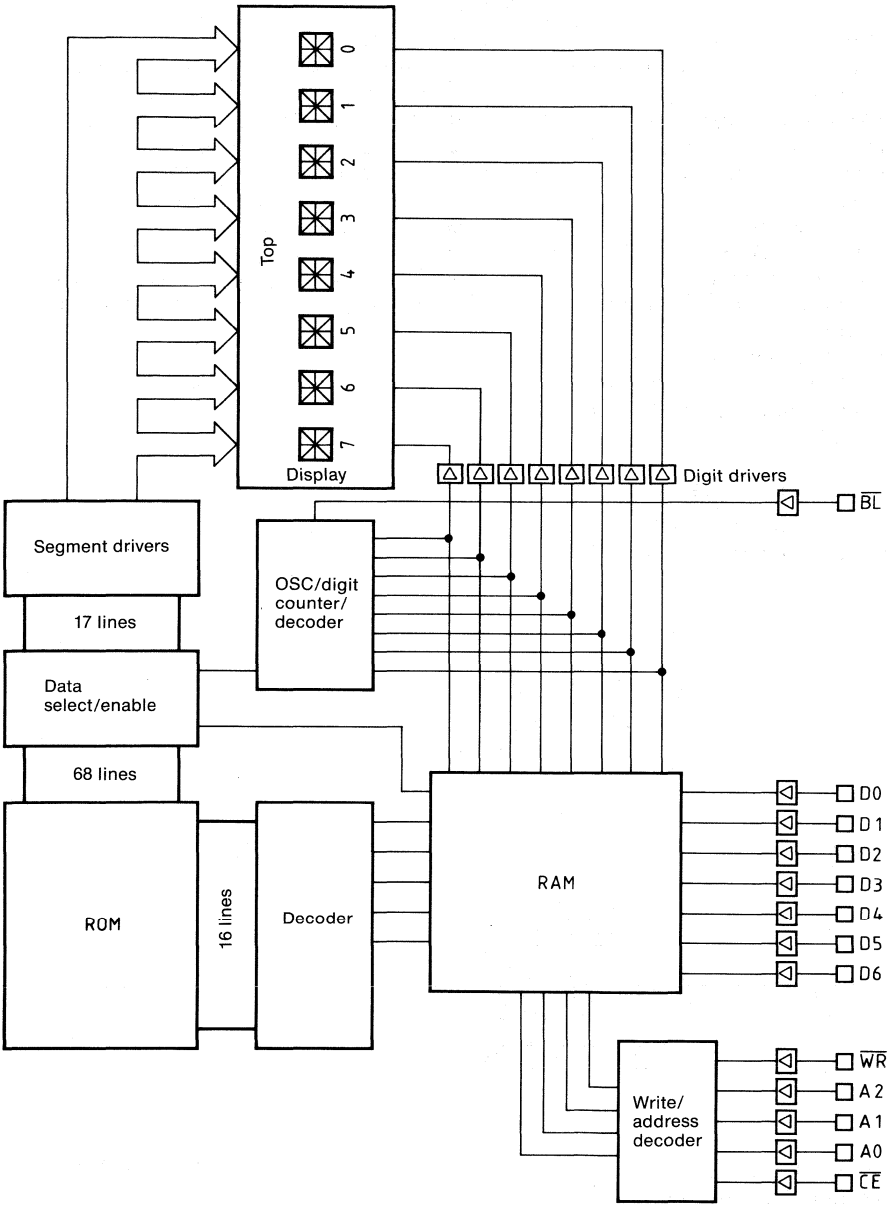
		D0	L	H	L	H	L	H	L	H
		D1	L	L	H	H	L	L	H	H
		D2	L	L	L	L	H	H	H	H
D6	D5	D4	D3								
L	H	L	L		!	"	#	$	%	&	'
L	H	L	H	(	)	*	+	,	-	.	/
L	H	H	L	0	1	2	3	4	5	6	7
L	H	H	H	8	9	:	;	<	=	>	?
H	L	L	L	@	A	B	C	D	E	F	G
H	L	L	H	H	I	J	K	L	M	N	O
H	L	H	L	P	Q	R	S	T	U	V	W
H	L	H	H	X	Y	Z	[	\	]	^	_

All other input codes display "Blank".

Loading data state table

			Address			Data input							Digit							
$\overline{BL}$	$\overline{CE}$	$\overline{WR}$	A2	A1	A0	D6	D5	D4	D3	D2	D1	D0	7	6	5	4	3	2	1	0
H	X	H	X	X	X	Previously loaded display							R	E	D	G	R	E	E	N
H	H	X	X	X	X	X	X	X	X	X	X	X	R	E	D	G	R	E	E	N
H	L	L	L	L	L	H	L	L	L	H	L	H	R	E	D	G	R	E	E	E
H	L	L	L	L	H	H	L	H	L	H	L	H	R	E	D	G	R	E	U	E
H	L	L	L	H	L	H	L	L	H	H	L	L	R	E	D	G	R	L	U	E
H	L	L	L	H	H	H	L	L	L	L	H	L	R	E	D	G	B	L	U	E
H	L	L	H	L	L	H	L	L	L	H	L	H	R	E	D	E	B	L	U	E
H	L	L	H	L	H	H	L	H	L	H	L	H	R	E	U	E	B	L	U	E
H	L	L	H	H	L	H	L	L	H	H	L	L	R	L	U	E	B	L	U	E
H	L	L	H	H	H	H	L	L	L	L	H	L	B	L	U	E	B	L	U	E
L	X	H	X	X	X	Blank display														
H	L	L	L	H	H	H	L	L	L	H	H	H	B	L	U	E	G	L	U	E
H	L	L	X	X	X	See character code								See character set						

Block diagram

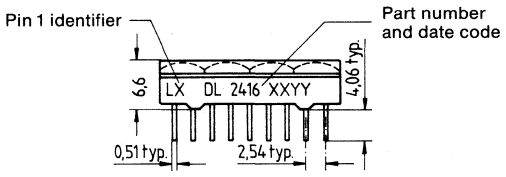


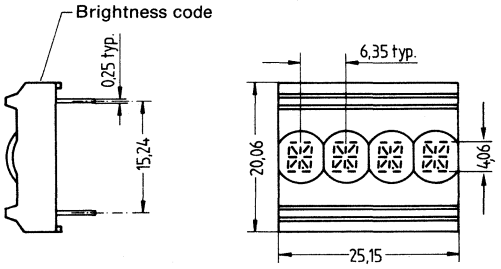
Alphanumeric intelligent displays with memory, decoder, and driver
4.1 mm, red, 4 digits, 16 segments plus decimal

Features

- 4.1 mm high, magnified monolithic characters
- Wide viewing angle, ± 50 degrees
- Close vertical row spacing, 20.3 mm
- Rugged, solid, plastic-encapsulated package
- Fast access time:
  DL 2416: 500 ns
  DL 2416 H: 300 ns
- Full-size display for stationary equipment
  - built-in memory
  - built-in character generator
  - built-in multiplex and LED drive circuitry
- Direct access to each digit independently and asynchronously
- TTL compatible, 5 V power supply
- Independent cursor function
- 17th segment for improved punctuation marks
- Display blank function
- Memory clear function
- End-stackable, four character package
- Intensity coded for display uniformity

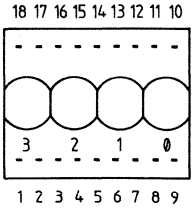
Type	Ordering code
DL 2416	Q68000-A5577-F114
DL 2416 H	Q68000-A6365-F114





Tolerance ± 0.25 mm,
unless otherwise specified

Dimensions in mm



Pin configuration (top view – display side)

Pin	Function	Pin	Function
1	$\overline{CE1}$ Chip enable	18	$\overline{BL}$ Display blank
2	$\overline{CE2}$ Chip enable	17	D4 Data input
3	$\overline{CLR}$ Clear	16	D5 Data input
4	CUE Cursor enable	15	D6 Data input
5	$\overline{CU}$ Cursor select	14	D3 Data input
6	$\overline{WR}$ Write	13	D2 Data input
7	A1 Digit select	12	D1 Data input
8	AØ Digit select	11	DØ Data input
9	V_{CC} Supply voltage +5 V	10	GND Ground (Ø V)

Description

The DL 2416 is a four digit display module having 16 segments plus decimal and a built-in CMOS integrated circuit.

The IC contains memory, ASCII ROM decoder, multiplexing circuitry, and drivers. Data entry is asynchronous and can be random. A display system can be built using any number of DL 2416s since each digit of any DL 2416 can be addressed independently and will continue to display the character last stored until replaced by another.

System interconnection is very straightforward. The least significant two address bits (AØ, A1) are normally connected to the like-named inputs of all DL 2416s in the system. With two chip enables ($\overline{CE1}$, and $\overline{CE2}$) four DL 2416s (16 characters) can easily be interconnected without a decoder.

Alternatively, one-of-n decoder ICs can be used to extend the address for large displays.

Data lines are connected to all DL 2416s directly and in parallel, as is the write line ($\overline{WR}$). The display will then behave as a write-only memory.

The cursor function causes all segments of a digit position to illuminate. The cursor is not a character, however, and upon removal the previously displayed character will reappear.

Optoelectronic characteristics at 25 °C

Maximum ratings

Voltage, any pin with respect to GND	−0.5 ... +6.0 V
Operating temperature	−20 ... +65 °C
Storage temperature	−20 ... +70 °C
Relative humidity at 65 °C (non-condensing)	85 %

Optical characteristics (typical)

Luminous intensity per digit/8 segments at 5 V	0.5 mcd
Viewing angle[1])	± 50 degrees
Spectral peak wavelength	660 nm
Digit size	4.06 mm

DC characteristics

Symbol	Parameter	−20 °C typ.	+25 °C[5])	+65 °C typ.	Test conditions
I_{CC}	V_{CC} supply current (10 segs/char., 4 digits on)	135 mA	125 mA max.[2])	100 mA	V_{CC} = 5.0 V
I_{CC}	V_{CC} supply current cursor[3])	160 mA	140 mA max.[2])	120 mA	V_{CC} = 5.0 V
I_{CC}	V_{CC} supply current (display blank)		3.7 mA max.		V_{IN} = 0 V V_{CC} = 5.0 V $\overline{WR}$ = 5.0 V
I_{IL}	Input current – low	200 µA	160 µA max.	100 µA	V_{IN} = 0.8 V V_{CC} = 5.0 V
V_{IL}	Input voltage – low		0.8 V max.		V_{CC} = 4.5 V
V_{IH}	Input voltage – high[4])		2.7 V min.		V_{CC} = 4.5 V
			3.3 V min.		V_{CC} = 5.5 V

[1]) "Off Axis Viewing Angle" is here defined as: "the minimum angle in any direction from the normal to the display surface at which any part of any segment in the display is not visible".

[2]) Measured at 5 s.

[3]) 60 s max. duration.

[4]) $V_{CC} \geqq V_{IH} \geqq 0.6 \cdot V_{CC}$.

[5]) V_{CC} = +5.0 V ±10 %.

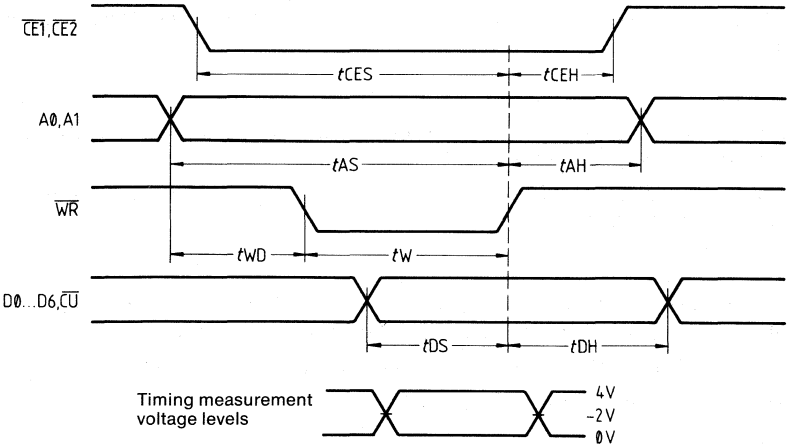
AC characteristics

Timing parameters at V_{CC} = 4.5 V (nanoseconds)

Symbol	Parameter	−20 °C typ.		+25 °C min.		+65 °C typ.	
		DL 2416	DL 2416 H	DL 2416	DL 2416 H	DL 2416	DL 2416 H
*t*AS	Address setup	300	200	450	250	600	400
*t*WD	Write delay	50	50	150	50	175	75
*t*W	Write pulse	250	150	300	200	425	325
*t*DS	Data setup	150	100	250	150	350	250
*t*DH	Data hold	50	50	50	50	100	100
*t*AH	Address hold	50	50	50	50	100	100
*t*CEH	Chip enable hold	50	50	50	50	100	100
*t*CES	Chip enable setup	300	150	450	250	600	400
*t*CLR	Clear			15 ms	15 ms		
				Access time			
				500 ns	300 ns		

Timing characteristics

Write cycle waveforms



Loading data

Setting the chip enables ($\overline{CE1}$, $\overline{CE2}$) to their true state will enable data loading. The desired data code (DØ...D6) and digit address (AØ, A1) must be held stable during the write cycle for storing new data.

Data entry may be asynchronous and random. (Digit Ø is defined as right hand digit with A1 = AØ = Ø.)

Clearing of the entire internal four-digit memory can be accomplished by holding the clear ($\overline{CLR}$) low for one complete display multiplex cycle, 15 ms minimum. Loading an illegal data code will display a blank.

Loading cursor

Setting the chip enables ($\overline{CE1}$, $\overline{CE2}$) and cursor select ($\overline{CU}$) to their true state will enable cursor loading. A write ($\overline{WR}$) pulse will now store or remove a cursor into the digit location addressed by AØ, A1; as defined in data entry. A cursor will be stored if DØ = 1; and will be removed if DØ = Ø. Cursor will **not** be cleared by the $\overline{CLR}$ signal. The cursor ($\overline{CU}$) pulse width should not be less than the write ($\overline{WR}$) pulse or erroneous data may appear in the display.

For those users not requiring the cursor, the cursor enable signal (CUE) may be tied low to disable display of the cursor function. A flashing cursor can be realized by simply pulsing CUE. If cursor has been loaded to any or all positions in the display, then CUE will control whether the cursor(s) or the characters appear. CUE does not affect the contents of cursor memory.

Blanking the display

Blanking the display may be accomplished by loading a blank or space into each digit of the display or by using the ($\overline{BL}$) display blank input.

Setting the ($\overline{BL}$) input low does not affect the contents of either data or cursor memory. A flashing display can be realized by pulsing ($\overline{BL}$).

Notes

1) This display contains a CMOS integrated circuit. Normal CMOS handling precautions should be taken to avoid damage due to high static voltages or electric fields.
2) Unused inputs must be tied to an appropriate logic voltage level (either V+ or V−).
3) **Warning:** Do not use solvents containing alcohol!

Loading data state table

Control							Address		Data input							Display digit			
$\overline{BL}$	$\overline{CE1}$	$\overline{CE2}$	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A1	AØ	D6	D5	D4	D3	D2	D1	DØ	3	2	1	Ø
H	X	X	L	X	H	H	Previously loaded display									G	R	E	Y
H	H	X	L	X	X	H	X	X	X	X	X	X	X	X	X	G	R	E	Y
H	X	H	L	X	X	H	X	X	X	X	X	X	X	X	X	G	R	E	Y
H	L	L	L	H	L	H	L	L	H	L	L	L	H	L	H	G	R	E	E
H	L	L	L	H	L	H	L	H	H	L	H	L	H	L	H	G	R	U	E
H	L	L	L	H	L	H	H	L	H	L	L	H	H	L	L	G	L	U	E
H	L	L	L	H	L	H	H	H	H	L	L	L	L	H	L	B	L	U	E
L	X	X	X	X	H	H	X	X	Blank display										
H	L	L	L	H	L	H	H	H	H	L	L	L	H	H	H	G	L	U	E
H	X	X	L	X	H	L	X	X	Clears character displays							see character set			
H	L	L	L	H	L	H	X	X	See character code										

X ≙ don't care

Loading cursor state table

Control							Address		Data input							Display digit			
$\overline{BL}$	$\overline{CE1}$	$\overline{CE2}$	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A1	AØ	D6	D5	D4	D3	D2	D1	DØ	3	2	1	Ø
H	X	X	L	X	H	H	Previously loaded display									B	E	A	R
H	X	X	H	X	H	H	Display previously stored cursors									B	E	A	R
H	L	L	H	L	L	H	L	L	X	X	X	X	X	X	H	B	E	A	⊠
H	L	L	H	L	L	H	L	H	X	X	X	X	X	X	H	B	E	⊠	⊠
H	L	L	H	L	L	H	H	L	X	X	X	X	X	X	H	B	⊠	⊠	⊠
H	L	L	H	L	L	H	H	H	X	X	X	X	X	L	H	⊠	⊠	⊠	⊠
H	L	L	H	L	L	H	H	L	X	X	X	X	X	X	L	⊠	E	⊠	⊠
H	X	X	L	X	H	H	Disable cursor display									B	E	A	R
H	L	L	L	L	L	H	H	H	X	X	X	X	X	X	L	B	E	A	R
H	X	X	H	X	H	H	Display stored cursor									B	E	⊠	⊠

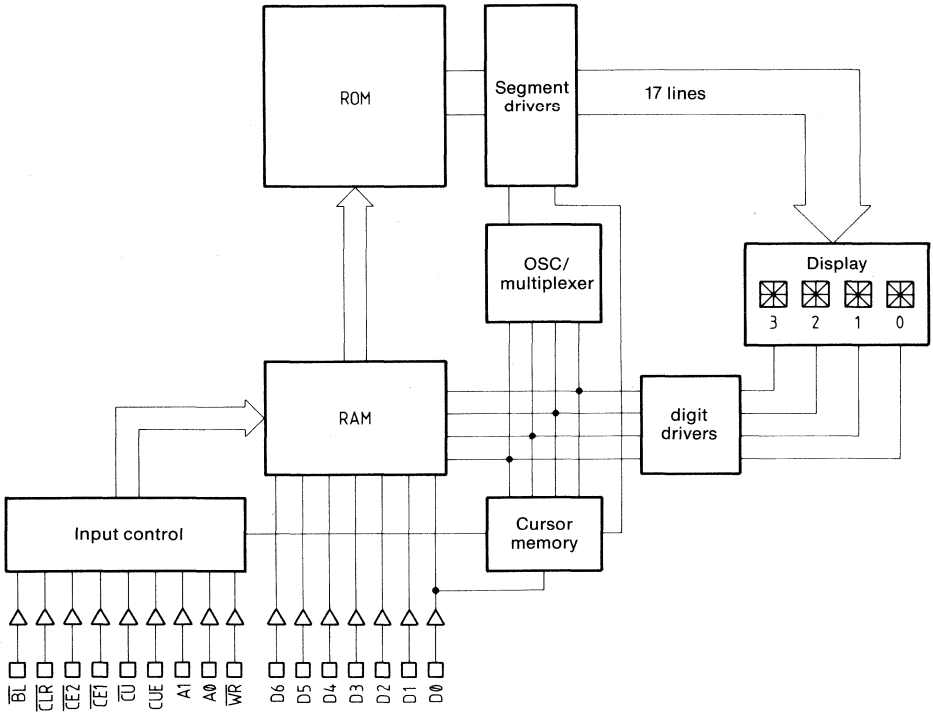
X ≙ don't care

Character set

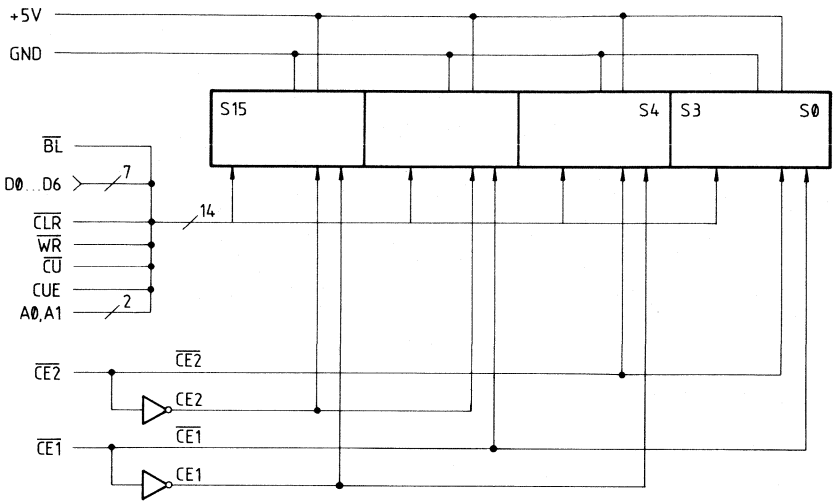
				D0	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
				D1	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
				D2	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
				D3	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
	D6	D5	D4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	L	H	L	2		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
	L	H	H	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
	H	L	L	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
	H	L	H	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_

All other input codes display "blank"

Block diagram



Typical schematic for 16-digit system

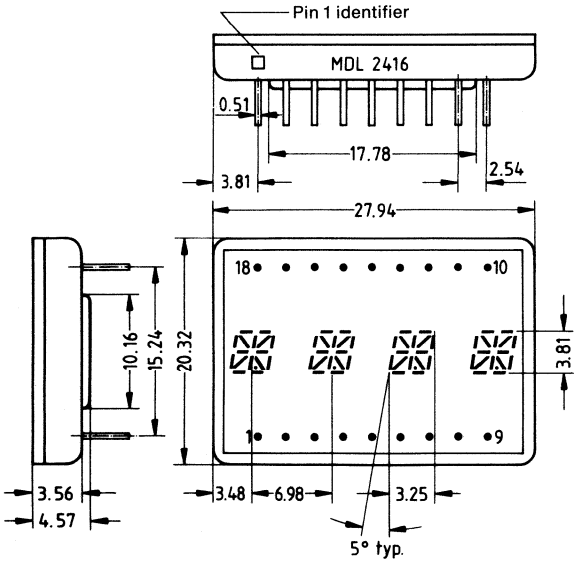


High rel military alphanumeric intelligent displays with memory, decoder, and driver. 3.81 mm, red, 4 digits, 16 segments plus decimal.

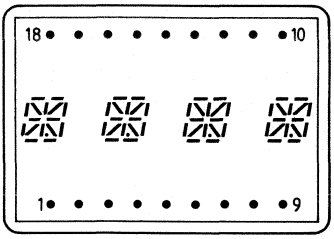
Features

- MDL 2416-B fully processed to MIL Standard 883/level B
- 3.81 mm high, non-magnified monolithic character
- Rugged metal can with hermetic sealed flat quartz lens
- Close vertical row spacing, 20.32 mm
- Wide viewing angle, ±50 degrees
- Wide operating temperature range for high rel industrial and military use
- Fully integrated CMOS drive electronics
- Direct access to each digit independently and asynchronously
- TTL compatible, 5 V power supply
- Independent cursor function
- 17th segment for improved punctuation marks
- Two chip enables
- Interdigit blank function
- Display blank function
- Memory clear function
- End-stackable, four character package
- Intensity coded for display uniformity
- Full dimming capability

Type	Ordering code
MDL 2416	Q68000–A7219–F114
MDL 2416-B	Q68000–A7309–F114



Dimensions in mm



Pin configuration (top view – display side)

Pin	Function	Pin	Function
1	$\overline{CE1}$ Chip enable	18	$\overline{BL}$ Display blank
2	$\overline{CE2}$ Chip enable	17	D4 Data input
3	$\overline{CLR}$ Clear	16	D5 Data input
4	CUE Cursor enable	15	D6 Data input
5	$\overline{CU}$ Cursor select	14	D3 Data input
6	$\overline{WR}$ Write	13	D2 Data input
7	A1 Digit select	12	D1 Data input
8	AØ Digit select	11	DØ Data input
9	V_{CC}	10	GND

Description

The MDL 2416 is a hi-rel four digit display having a 17 segment font and built-in CMOS drive circuitry that is TTL and microprocessor compatible. The integrated circuit contains memory, ASCII ROM decoder, multiplexing circuitry, and drivers. Data entry is asynchronous and can be random. A display system can be built using any number of MDL 2416s since each digit of any MDL 2416 can be addressed independently and will continue to display the character last stored until replaced by another.

Loading data

System interconnection is straightforward. The least significant two address bits (AØ, A1) are normally connected to the like-named inputs of all MDL 2416s in the system. With two chip enables ($\overline{CE1}$, $\overline{CE2}$), two MDL 2416s (8 characters) can easily be interconnected without an external decoder.

Setting the chip enables ($\overline{CE1}$, $\overline{CE2}$) to their true state will enable data loading. The desired data code (DØ...D6) and digit address (AØ, A1) must be held stable during the write cycle for storing new data. Data entry may be asynchronous and random. (Digit Ø is defined as right hand digit with A1 = AØ = Ø.)

Clearing of the entire internal four digit memory can be accomplished by holding the clear ($\overline{CLR}$) low for one complete display multiplex cycle, 15 ms minimum. Loading an illegal data code will display a blank.

Loading cursor

Setting the chip enables ($\overline{CE1}$, $\overline{CE2}$) and cursor select ($\overline{CU}$) to their true state will enable cursor loading. A write ($\overline{WR}$) pulse will now store or remove a cursor into the digit location addressed by AØ, A1; as defined in data entry. A cursor will be stored if DØ = 1; and will be removed if DØ = Ø. Cursor will not be cleared by the $\overline{CLR}$ signal. The cursor ($\overline{CU}$) pulse width should not be less than the write ($\overline{WR}$) pulse or erroneous data may appear in the display.

For those users not requiring the cursor, the cursor enable signal (CUE) may be tied low to disable display of the cursor function. A flashing cursor can be realized by simply pulsing CUE. If cursor has been loaded to any or all positions in the display, then CUE will control whether the cursor(s) or the characters appear. CUE does not affect the contents of the cursor memory.

Blanking display

Blanking the display may be accomplished by loading a blank or space into each digit of the display or by using the ($\overline{BL}$) display blank input.

Setting the ($\overline{BL}$) input low does not affect the contents of either data or cursor memory. A flashing display can be realized by pulsing ($\overline{BL}$). For dimming, see note 6.

Optoelectronic characteristics at 25 °C

Maximum ratings

Voltage, any pin with respect to GND	−0.5... +6.0 V
Operating temperature (note 1)	−55 ... +100 °C
Storage temperature	−55 ... +125 °C
Relative humidity at 85 °C (non-condensing)	85 %

Optical characteristics (typical)

Luminous intensity (at V_{CC} = 5 V)	0.1 mcd/seg.
Viewing angle (note 2)	±50 degrees
Digit size	3.81 mm
Spectral peak wavelength (typ.)	660 nm

DC characteristics

Symbol	Parameter	min.	typ.	max.	Test conditions
I_{CC}	V_{CC} supply current		12.0 mA	19.0 mA	V_{CC} = 5 V, $\overline{WR} = V_{CC}$, V_{IN} = Ø V, (display blank)
I_{CC}	V_{CC} supply current		125 mA	150 mA	V_{CC} = 5 V, (10 segs/char., 4 digits on)
I_{CC}	V_{CC} supply current		150 mA max.	175 mA	V_{CC} = 5 V, 5 sec. max. (all segments on, cursor in 4 digits)
V_{IL}	Input voltage – low (all inputs)			0.8 V	V_{CC} = 5 V
V_{IH}	Input voltage – high (all inputs)	3.0 V			V_{CC} = 5 V
I_{IL}	Input current – low (all inputs)			160 µA	V_{CC} = 5 V, V_{IN} = 0.8 V

AC characteristics at 25 °C

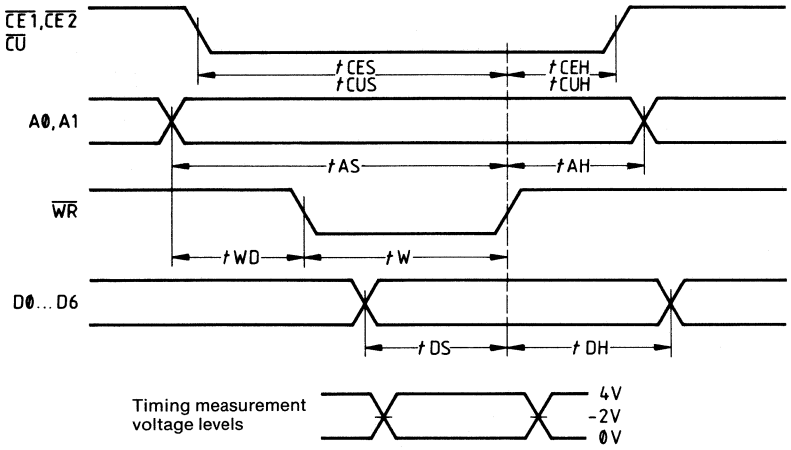
Minimum timing parameters at V_{CC} = 4.5 V (nanoseconds)

Symbol	Parameter	min. at +25 °C	min. at +100 °C	unit
*t*WD	Write delay	150	175	ns
*t*AS	Address setup	450	600	ns
*t*CES	Chip enable setup	450	600	ns
*t*CEH	Chip enable hold	50	50	ns
*t*DS	Data setup	250	350	ns
*t*W	Write pulse	300	425	ns
*t*AH	Address hold	50	50	ns
*t*DH	Data hold	50	50	ns
*t*CLR	Clear	15	15	ms
*t*CUS	Cursor enable setup	450	600	ns
*t*CUH	Cursor enable hold	50	50	ns

Timing parameters at −55 °C will be defined.

Timing characteristics

Write cycle waveforms



Character set

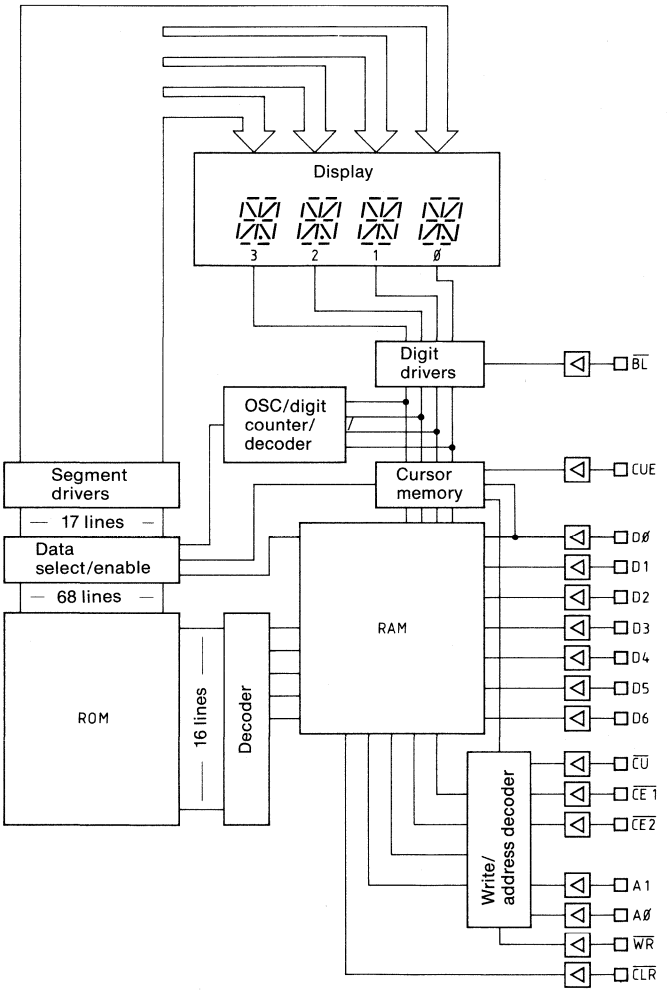
				D0	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
				D1	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
				D2	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
				D3	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
	D6	D5	D4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
	L	H	L	2		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
	L	H	H	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
	H	L	L	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
	H	L	H	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_

All other input codes display blank

Notes

1) Present maximum operating temperature is 100°C. After evaluation, maximum operating temperature may be raised to 125°C.
2) "Off Axis Viewing Angle" is here defined as "the minimum angle in any direction from the normal to the display surface at which any part of any segment in the display is not visible".
3) This display contains a CMOS IC. Normal CMOS handling precautions should be taken to avoid damage due to high static voltages or electric fields. See "Guidelines for Handling and Using Intelligent Displays".
4) Unused inputs must be tied to an appropriate logic voltage level (either V+ or V−).
5) Cursors displayed in all character positions should not remain on any longer than 60 seconds.
6) Dimming is accomplished by varying a pulse width on the blanking pin.

Block diagram



Appendix "G" for class B (MIL-M-38510)
(MIL-Std-883B, method 5008)

Group B tests

Screen	Method	Reqmt.	Comments
Physical dimensions	2016	100 %	
Resistance to solvents	2015	Sample	
Internal visual and mechanical examination	2014	100 %	
Bond strength	2011	Sample	
Die shear strength	2019	Sample	
Solderability	2003	Sample	Soldering temperature of 260 °C ±10 °C

Group C tests

Screen	Method	Reqmt.	Comments
Temperature cycling	1010, test condition C	100 %	10 cycles −65 °C to +150 °C 10 min. at each extreme value
Constant acceleration	2001, test condition A	100 %	Y1 and Y2 orientation
Seal (a) Fine (b) Gross	1014 Cond. A1 Cond. C	100 %	60 PSIG 2 hrs. FC-40 at 125 °C 30 sec
Visual examination	For catastrophic failures	100 %	
End point electrical parameters	(Group A tests)	100 %	As specified in the applicable device specification
Burn-in	1015 Cond. B	100 %	Test condition to be specified is the applicable procurement document (160 hrs. at 100 °C see note 1)

Application Notes Intelligent Display DL 2416 with Microprocessors

This application note is intended to serve as a design and application guide for users of the DL 2416 alphanumeric intelligent display.

The information presented covers:
device electrical description and operation,
considerations for general circuit design,
interfacing the DL 2416 to microprocessors.

Electrical and mechanical description

General

The internal electronics in the DL 2416 intelligent display eliminates all the traditional difficulties of using multi-digit light emitting displays (segment decoding, drivers, and multiplexing). The intelligent display also provides internal memory for the four digits. This approach allows the user to asynchronously address one of four digits, and load new data regardless of the LED multiplex timing.

Figure 1 is a block diagram of the DL 2416. The unit consists of four 17 segment monolithic LED die and a single CMOS integrated circuit chip. The LED die are magnified to a height of 4.1 mm by built-in lenses. The IC chip contains 17 segment drivers, four digit drivers, 64 character ROM, four word × 7 bit Random Access Memory, oscillator for multiplexing, multiplex counter/decoder, cursor memory, address decoder, and miscellaneous control logic.

Packaging

Packaging consists of a transfer-molded lexan or nylon lens which also serves as an "encapsulation shell" since it covers five of the six "faces". The assembled and tested substrate (ceramic or "PTF" multilayer), is placed within the shell and the entire assembly is then filled with a water-clear IC-grade epoxy.

This yields a very rugged part, which is quite impervious to moisture, shock and vibration. Although not "hermetic", the device will easily withstand total immersion in water/detergent solutions.

Figure 1
Block diagram

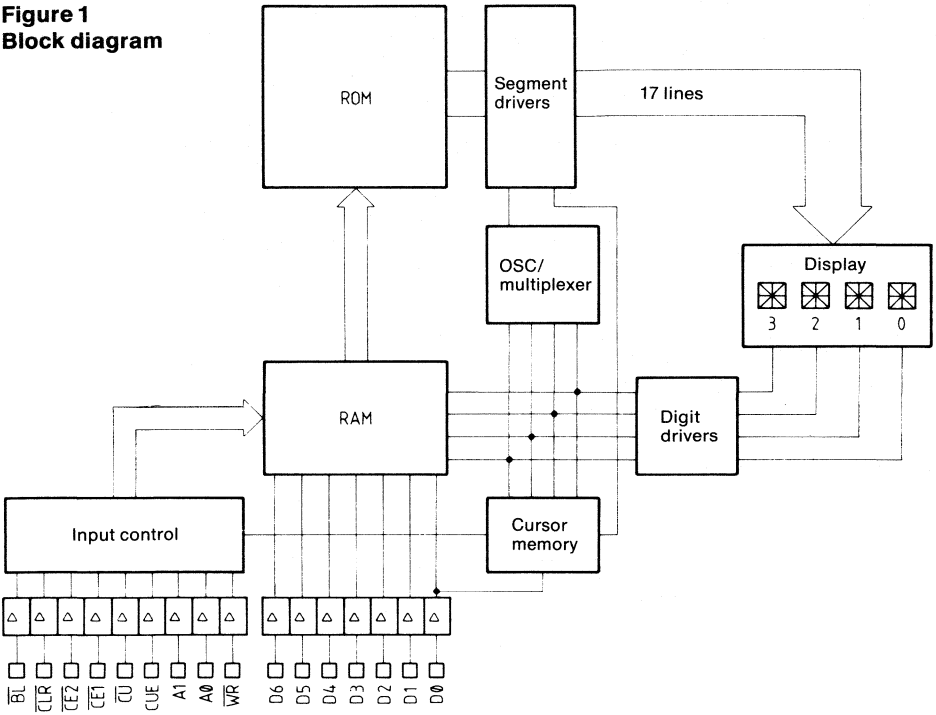
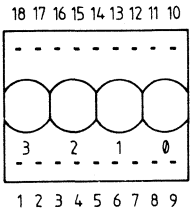


Figure 2
Pin configuration (top view – display side)



Pin	Function	Pin	Function
1	$\overline{CE1}$ Chip enable	18	$\overline{BL}$ Display blank
2	$\overline{CE2}$ Chip enable	17	D4 Data input
3	$\overline{CLR}$ Clear	16	D5 Data input
4	CUE Cursor enable	15	D6 Data input
5	$\overline{CU}$ Cursor select	14	D3 Data input
6	$\overline{WR}$ Write	13	D2 Data input
7	A1 Chip select	12	D1 Data input
8	AØ Chip select	11	DØ Data input
9	V_{CC} +5 V power supply	10	GND Ground (Ø V)

Electrical inputs to the DL 2416

V_{CC} Positive supply +5 V

GND Ground

DØ...D6 Data lines
The seven data input lines are designed to accept the first 64 ASCII characters. See **figure 3** for character set. (The DL 2416 interprets all undefined codes as a blank).

AØ, A1 Address lines
The address determines the digit position to which the data will be written. Address order is right to left for positive-true logic.

$\overline{WR}$ Write (active low)
Data and address to be loaded must be present and stable before and after the trailing edge of write. (See data sheet for timing information.)

$\overline{CE1}$, $\overline{CE2}$ Chip enable (active low)
This determines which device in an array will actually accept data. When either or both chip enable is in the high state, all inputs are inhibited.

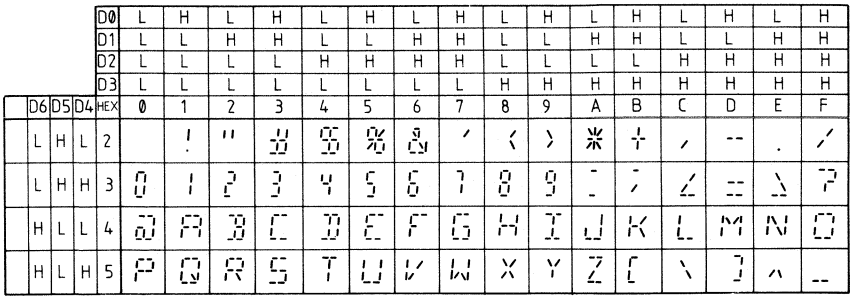
$\overline{CLR}$ Clear (active low)
When held low for 15 ms, the data RAM will be cleared.

CUE Cursor enable, activates cursor function
Cursor will not be displayed regardless of cursor memory contents when CUE is low.

$\overline{CU}$ Cursor select (active low)
This input must be held high to store data in data memory and low to store data into the cursor memory.

$\overline{BL}$ Display blank (active low)
Blanking the entire display may be accomplished by holding the $\overline{BL}$ input low. This is not a stored function, however. When $\overline{BL}$ is released, the stored characters are again displayed.

Figure 3
Character set



Clear memory

Clearing of the entire internal four-digit memory may be accomplished by holding the clear line ($\overline{CLR}$) low for one complete internal display multiplex cycle, 15 ms minimum; less time may leave some data uncleared. $\overline{CLR}$ does not clear the cursor memory.

Display blanking

Blanking the display may be accomplished by loading a blank, space or illegal code into each digit of the display or by using the ($\overline{BL}$) display blank input. Setting the ($\overline{BL}$) input low does not affect the contents of either data or cursor memory. A flashing display can be realized by pulsing ($\overline{BL}$).

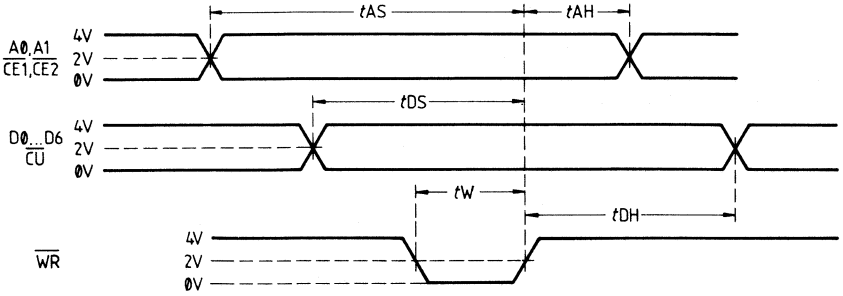
Operation

Multiplexed display systems sequentially read and display data from a memory device. In synchronous systems, control circuitry must compare the location of data to be read to the location or position of new data to be stored or displayed, i.e., synchronize before a write can be done. This can be slow and cumbersome.

Data entry in "intelligent displays" is asynchronous and may be done in any random order. Loading data is similar to writing into a RAM. Each digit has its own memory location and will display until replaced by another code.

The waveforms of **figure 4** demonstrate the relationships of the signals required to generate a write cycle. (Check individual data sheet for minimum values.) As can be seen from the waveforms, all signals are referenced from the rising or trailing edge of write.

Figure 4
Timing characteristics (write cycle waveforms)



Cursor

The cursor function causes all 16 line-segments of a digit to light. The cursor can be used to indicate the position in the display of the next character to be entered. The cursor is not a character but overrides the display of a stored character. Upon removal of the cursor, the display will again show the character stored in memory.

The cursor can be written into any digit position by setting the cursor enable (CUE) high, setting the digit address (A1, AØ), enabling chip enable, ($\overline{CE1}$, $\overline{CE2}$), cursor select ($\overline{CU}$), write ($\overline{WR}$) and data (DØ). A high on data line DØ will place a cursor into the position set by the address AØ and A1. Conversely, a low on DØ will remove the cursor. The cursor will remain displayed after the cursor ($\overline{CU}$) and write ($\overline{WR}$) signals have been removed. During the cursor-write sequence, data lines D1 through D6 are ignored by the DL 2416.

If the user does not wish to utilize the cursor function, the cursor enable (CUE) can be tied low to disable the cursor function. A flashing cursor can be realized by simply pulsing the CUE line after cursor data has been stored.

Figure 5
Loading data

Control							Address		Data							Digit			
$\overline{BL}$	$\overline{CE1}$	$\overline{CE2}$	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A1	AØ	D6	D5	D4	D3	D2	D1	DØ	3	2	1	Ø
L	X	X	X	H	X	H	X	X	X	X	X	X	X	X	X	"Blank"			
H	H	X	L	H	X	H	X	X	X	X	X	X	X	X	X	previous characters			
H	X	H	L	H	X	H	X	X	X	X	X	X	X	X	X	NC	NC	NC	NC
H	X	X	L	H	H	H	X	X	X	X	X	X	X	X	X	NC	NC	NC	NC
H	L	L	L	H	L	H	L	L	H	L	L	L	L	L	H	NC	NC	NC	A
H	L	L	L	H	L	H	L	H	H	L	L	L	L	H	L	NC	NC	B	A
H	L	L	L	H	L	H	H	L	H	L	L	L	L	H	H	NC	C	B	NC
H	L	L	L	H	L	H	H	H	H	L	L	L	H	L	L	D	C	NC	A
H	L	L	L	H	L	H	L	L	H	L	L	L	H	L	H	D	C	B	E
H	L	L	L	H	L	H	H	L	H	L	L	H	L	H	H	D	K	B	E
H	L	L	L	H	L	H	—	—	—	—	—	—	—	—	—				

X ≙ don't care, NC ≙ no change from previously displayed characters

Loading cursor

Control							Address		Data							Digit			
$\overline{BL}$	$\overline{CE1}$	$\overline{CE2}$	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A1	AØ	D6	D5	D4	D3	D2	D1	DØ	3	2	1	Ø
H	L	L	L	H	X	H	X	X	X	X	X	X	X	X	X	Normal data entry			
H	L	L	H	H	H	H	X	X	X	X	X	X	X	X	X	Enable previously stored cursors			
H	L	L	H	L	L	H	L	L	X	X	X	X	X	X	H	NC	NC	NC	⊠
H	L	L	H	L	L	H	L	H	X	X	X	X	X	X	H	NC	NC	⊠	⊠
H	L	L	H	L	L	H	H	L	X	X	X	X	X	X	H	NC	⊠	⊠	⊠
H	L	L	H	L	L	H	H	H	X	X	X	X	X	X	H	⊠	⊠	⊠	⊠
H	L	L	L	H	H	H	X	X	X	X	X	X	X	X	X	D	K	B	E
H	L	L	L	L	L	H	L	L	X	X	X	X	X	X	L	D	K	B	E
H	L	L	H	H	H	H	X	X	X	X	X	X	X	X	X	⊠	⊠	⊠	E

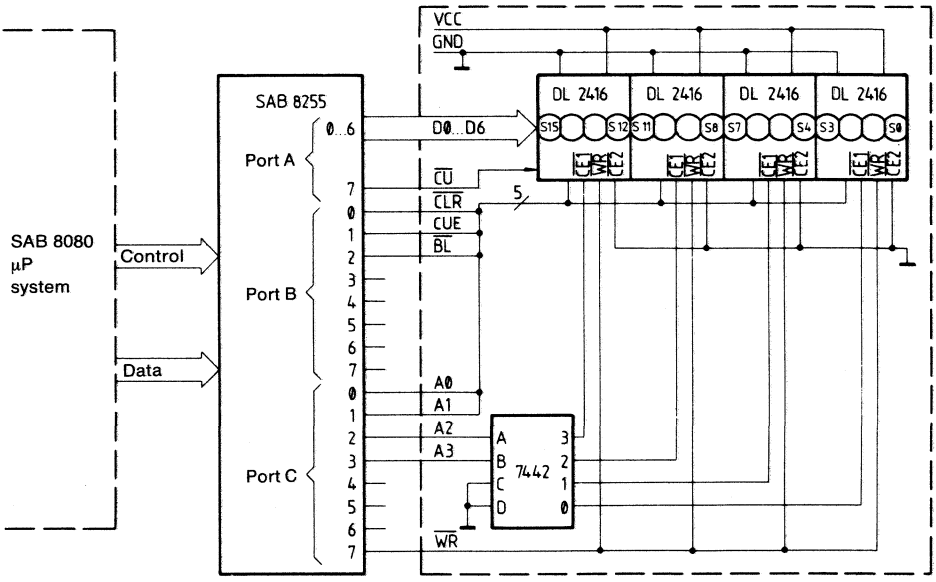
X ≙ don't care, NC ≙ no change from previously displayed characters

Parallel I/O

The parallel I/O device of a microprocessor can easily be connected to the circuit in **figure 6**. One eight-bit output port can provide the seven input data bits and the cursor ($\overline{CU}$). Another eight bit output port can contain the address and chip enable information and the other control signals.

Figure 7 illustrates a 16-character display with an 8080 system using the SAB 8255 programmable peripheral interface I/O device. The following program will display a simple 16-character message using this interface.

Figure 7
16-digit parallel I/O system



Sample I/O program

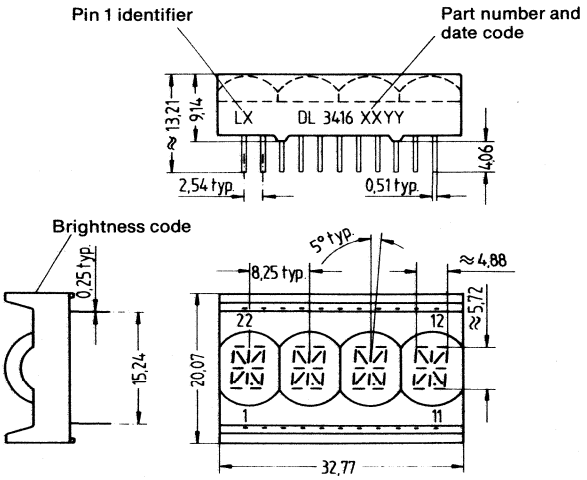
```
INIT:   MVI   A, 80H    ; Control data mode 0
        OUT   CONTROL   ; Load control register
CUSR:   MVI   A, 00H    ; Clear cursor data
        OUT   PORT A    ; Load data port
        MVI   B, 0FH    ; Set character counter
CUSRI:  MOV   A, B      ;
        CALL  DSPWT     ; Write subroutine
        DCR   B         ; Decrement counter
        JNZ   CUSRI     ; Digit 0?
        MOV   A, B      ;
        CALL  DSPWT     ;
        MVI   A, FFH    ; Set data for control
        OUT   PORT B    ; Load control lines
DISP:   LXI   H, TABLE  ; Set table address
DISP1:  MOV   A, M      ; Move table data into accumulator
        OUT   PORT A    ; Load data port
        MOV   A, B      ;
        CALL  DSPWT     ; Load address and control
        INX   H         ; Increment table address
        INR   B         ; Increment counter
        MVI   A, 10H    ; Set # of digits
        CMP   B         ;
        JNZ   DISP1     ; 16 characters?
        HALT            ; End of program
DSPWT:  ORI   F0H       ; Set control bits off
        OUT   PORT C    ; Load control
        ANI   7FH       ; Set write bit on
        OUT   PORT C    ; Load write
        ORI   F0H       ; Set write bit off
        OUT   PORT C    ; Load control
        RET             ;
TABLE:  DB              ; 0C3H
        DB              ; 0C9H
        DB              ; 0D4H
        DB              ; 0D3H
        DB              ; 0C1H
        DB              ; 0D4H
        DB              ; 0CEH
        DB              ; 0C1H
        DB              ; 0C6H
        DB              ; 0A0H
        DB              ; 0D3H
        DB              ; 0D4H
        DB              ; 0C8H
        DB              ; 0C7H
        DB              ; 0C9H
        DB              ; 0CCH
```

Alphanumeric intelligent displays with memory, decoder, and driver.
5.7 mm, red, 4 digits, 16 segments plus decimal

Features

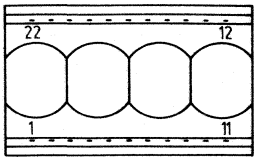
- 5.7 mm high, magnified monolithic characters
- Wide viewing angle, ±40 degrees
- Close vertical row spacing, 20.3 mm
- Rugged solid plastic-encapsulated package
- Fast access time:
  DL 3416: 500 ns
  DL 3416 H: 300 ns
- Full size display for stationary equipment
- Built-in memory
- Built-in character generator
- Built-in multiplex and LED drive circuitry
- Each digit independently addressed
- TTL compatible, 5 V power supply
- Independent cursor function
- 17th segment for improved punctuation marks
- Memory clear function
- Display blank function
- End-stackable, 4 character package
- Intensity coded for display uniformity

Type	Ordering code
DL 3416	Q68000-A6366-F114
DL 3416 H	Q68000-A6367-F114



Tolerance: ±0.25 mm,
unless otherwise specified

Dimensions in mm



Pin configuration (top view – display side)

Pin	Function	Pin	Function
1	CE1 Chip enable	22	D6 Data input
2	CE2 Chip enable	21	D5 Data input
3	$\overline{\text{CE3}}$ Chip enable	20	D4 Data input
4	$\overline{\text{CE4}}$ Chip enable	19	D3 Data input
5	$\overline{\text{CLR}}$ Clear	18	D2 Data input
6	V_{CC} Supply voltage	17	D1 Data input
7	AØ Digit select	16	DØ Data input
8	A1 Digit select	15	No connection
9	$\overline{\text{WR}}$ Write	14	$\overline{\text{BL}}$ Blanking
10	$\overline{\text{CU}}$ Cursor select	13	No connection
11	CUE Cursor enable	12	GND Ground

Description

The DL 3416 is a four digit display module having 16 segments plus decimal and a built-in CMOS IC.

The IC contains memory, ASCII ROM decoder, multiplexing circuitry, and drivers. Data entry is asynchronous and can be random. A display system can be built using any number of DL 3416s since each digit of any DL 3416 can be addressed independently and will continue to display the character last stored until replaced by another.

System interconnection is very straightforward. The least significant two address bits (AØ, A1) are normally connected to the like named inputs of all DL 3416s in the system. With four chip enables four DL 3416s (16 characters) can easily be interconnected without a decoder.

Loading data

Setting the chip enables (CE1, CE2, $\overline{CE3}$, $\overline{CE4}$) to their true state will enable data loading. The desired data code (DØ... D6) and digit address (AØ, A1) should be held stable during the write cycle for storing new data.

Data entry may be asynchronous and random. (Digit Ø is defined as right hand digit with A1 = AØ = Ø.)

Clearing of the entire internal four-digit memory can be accomplished by holding the clear ($\overline{CLR}$) low for one complete display multiplex cycle, 15 ms minimum.

Loading cursor

Setting the chip enables (CE1, CE2, $\overline{CE3}$, $\overline{CE4}$) and cursor select ($\overline{CU}$) to their true state will enable cursor loading. A write ($\overline{WR}$) pulse will now store or remove a cursor into the digit location addressed by AØ, A1; as defined in data entry. A cursor will be stored if DØ = 1; and will be removed if DØ = Ø. Cursor will **not** be cleared by the $\overline{CLR}$ signal. The cursor ($\overline{CU}$) pulse width should not be less than the write pulse ($\overline{WR}$) width or erroneous data may appear in the display.

For those users not requiring the cursor, the cursor enable signal (CUE) may be tied low to disable display of the cursor function. A flashing cursor can be realized be simply pulsing CUE. If cursor has been loaded to any or all positions in the display, then CUE will control whether the cursor(s) or the characters appear. CUE does not affect the contents of cursor memory.

Display blanking

Blanking the display may be accomplished by loading a blank or space into each digit of the display or by using the ($\overline{BL}$) display blank input.

Setting the ($\overline{BL}$) input low does not affect the contents of either data or cursor memory. A flashing display can be realized by pulsing ($\overline{BL}$).

Notes

1) This display contains a CMOS IC. Normal CMOS handling precautions should be taken to avoid damage due to high static voltages or electric fields.
2) Unused inputs must be tied to an appropriate logic voltage level (either V+ or V−).
3) **Warning** – Do not use solvents containing alcohol!

Loading data state table

Control									Address		Data input							Digit			
$\overline{BL}$	CE1	CE2	$\overline{CE3}$	$\overline{CE4}$	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A1	AØ	D6	D5	D4	D3	D2	D1	DØ	3	2	1	Ø
H	X	X	X	X	L	X	H	H	Previously loaded display									G	R	E	Y
H	L	X	X	X	L	X	X	H	X	X	X	X	X	X	X	X	X	G	R	E	Y
H	X	L	X	X	L	X	X	H	X	X	X	X	X	X	X	X	X	G	R	E	Y
H	X	X	H	X	L	X	X	H	X	X	X	X	X	X	X	X	X	G	R	E	Y
H	X	X	X	H	L	X	X	H	X	X	X	X	X	X	X	X	X	G	R	E	Y
H	X	X	X	X	L	X	H	H	X	X	X	X	X	X	X	X	X	G	R	E	Y
H	H	H	L	L	L	H	L	H	L	L	H	L	L	L	H	L	H	G	R	E	E
H	H	H	L	L	L	H	L	H	L	H	H	L	H	L	H	L	H	G	R	U	E
H	H	H	L	L	L	H	L	H	H	L	H	L	L	H	H	L	L	G	L	U	E
H	H	H	L	L	L	H	L	H	H	H	H	L	L	L	L	H	L	B	L	U	E
L	X	X	X	X	X	X	H	H	X	X	Blank display										
H	H	H	L	L	L	H	L	H	H	H	H	L	L	L	L	H	H	H	G	L	U	E
H	X	X	X	X	L	X	X	L	Clears character display									See character set			
H	H	H	L	L	L	H	L	H	X	X	See character code										

X = don't care

Loading cursor state table

Control									Address		Data input							Digit			
$\overline{BL}$	CE1	CE2	$\overline{CE3}$	$\overline{CE4}$	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A1	AØ	D6	D5	D4	D3	D2	D1	DØ	3	2	1	Ø
H	X	X	X	X	L	X	H	H	Previously loaded display									B	E	A	R
H	X	X	X	X	H	X	H	H	Display previously stored cursors									B	E	A	R
H	H	H	L	L	H	L	L	H	L	L	X	X	X	X	X	X	H	B	E	A	⊠
H	H	H	L	L	H	L	L	H	L	H	X	X	X	X	X	X	H	B	E	⊠	⊠
H	H	H	L	L	H	L	L	H	H	L	X	X	X	X	X	X	H	B	⊠	⊠	⊠
H	H	H	L	L	H	L	L	H	H	H	X	X	X	X	X	L	H	⊠	⊠	⊠	⊠
H	H	H	L	L	H	L	L	H	H	L	X	X	X	X	X	X	L	⊠	E	⊠	⊠
H	X	X	X	X	L	X	H	H	Disable cursor display									B	E	A	R
H	H	H	L	L	L	L	L	H	H	H	X	X	X	X	X	X	L	B	E	A	R
H	X	X	X	X	H	X	H	H	Display stored cursors									B	E	⊠	⊠

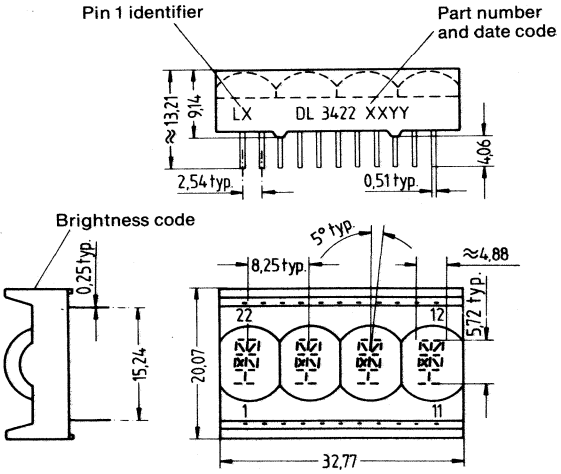
X = don't care

Alphanumeric intelligent display with memory, decoder, and driver.
4.3 mm/2.5 mm (nom.) upper and lower case letters, red, 4 digits, 22 segments.

Features

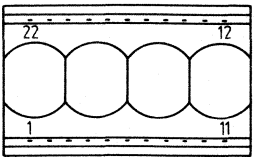
- 4.32 mm/2.54 mm (nom.) upper and lower case letters
- Wide viewing angle ±50 degrees
- Close vertical row spacing, 20.3 mm
- Rugged solid plastic encapsulated package
- Fast access time: 500 ns
- Fully size display for stationary equipment
- Built-in memory
- Built-in character generator
- Built-in multiplex and LED drive circuitry
- Direct access to each digit independently and asynchronously
- TTL compatible, 5 V power supply
- Independent cursor function
- 22 segments for 96 character ASCII format upper and lower case letters
- Memory clear function
- Display blank function

Type	Ordering code
DL 3422	Q68000–A6378–F114



Tolerance: ±0.25,
unless otherwise specified

Dimensions in mm



Pin configuration (top view – display side)

Pin	Function	Pin	Function
1	CE1 Chip enable	22	D6 Data input
2	No connection	21	D5 Data input
3	$\overline{CE2}$ Chip enable	20	D4 Data input
4	No connection	19	D3 Data input
5	$\overline{CLR}$ Clear	18	D2 Data input
6	V_{CC} Supply voltage, 5 V	17	D1 Data input
7	AØ Digit select	16	DØ Data input
8	A1 Digit select	15	No connection
9	$\overline{WR}$ Write	14	$\overline{BL}$ Blanking
10	$\overline{CU}$ Cursor select	13	No connection
11	CUE Cursor enable	12	GND Ground

Description

The DL3422 is a four digit display module having 22 segments and a built-in CMOS integrated circuit.

The IC contains memory, ASCII ROM decoder, multiplexing circuitry, and drivers. Data entry is asynchronous and can be random. A display system can be built using any number of DL 3422s since each digit of any DL 3422 can be addressed independently and will continue to display the character last stored until replaced by another.

System interconnection is very straightforward. The least significant two address bits (AØ, A1) are normally connected to the like named inputs of all DL 3422s in the system. With two chip enables (CE1, and $\overline{CE2}$) four DL 3422s (16 characters) can easily be interconnected without a decoder.

Alternatively, one-of-n decoder ICs can be used to extend the address for large displays.

Data lines are connected to all DL 3422s directly and in parallel, as is the write line ($\overline{WR}$). The display will then behave as a write-only memory.

The cursor function causes all segments of a digit position to illuminate. The cursor is **not** a character, however, and upon removal the previously displayed character will reappear.

Optoelectronic characteristics at 25 °C

Maximum ratings

Voltage, any pin with respect to GND	−0.5 ... +6.0 V
Operating temperature	−20 ... +65 °C
Storage temperature	−20 ... +70 °C
Relative humidity at 65 °C (non-condensing)	85 %

Optical characteristics (typical)

Luminous intensity (V_{CC} = 5.0 V) 8 segments/digit	0.5 mcd
Viewing angle[1])	±50 degrees
Peak wavelength	660 nm
Digit size	4.06 mm

DC characteristics

Symbol	Parameter	−20 °C typ.	+25 °C[5])	+65 °C typ.	Test conditions
I_{CC}	V_{CC} supply current 4 digits on (10 segments/digit)	135 mA	125 mA max.[2])	100 mA	V_{CC} = 5.0 V
I_{CC}	V_{CC} supply current[3]) (4 digits or cursor)	160 mA	140 mA max.[2])	120 mA	V_{CC} = 5.0 V
I_{CC}	V_{CC} supply current (display blank)		3.7 mA max.		V_{IN} = 0 V V_{CC} = 5.0 V $\overline{WR}$ = 5.0 V
I_{IL}	Input current – low	200 µA	160 µA max.	100 µA	V_{IN} = 0.8 V V_{CC} = 5.0 V
V_{IL}	Input voltage – low		0.8 V max.		V_{CC} = 4.5 V
V_{IH}	Input voltage – high[4])		2.7 V min.		V_{CC} = 4.5 V
			3.3 V min.		V_{CC} = 5.5 V

[1]) "Off Axis Viewing Angle" is here defined as: "the minimum angle in any direction from the normal to the display surface at which any part of the segment in the display is not visible".

[2]) Measured at 5 s.

[3]) 60 s max. duration.

[4]) $V_{CC} \geqq V_{IH} \geqq 0.6 \cdot V_{CC}$.

[5]) V_{CC} = +5.0 V ±10 %.

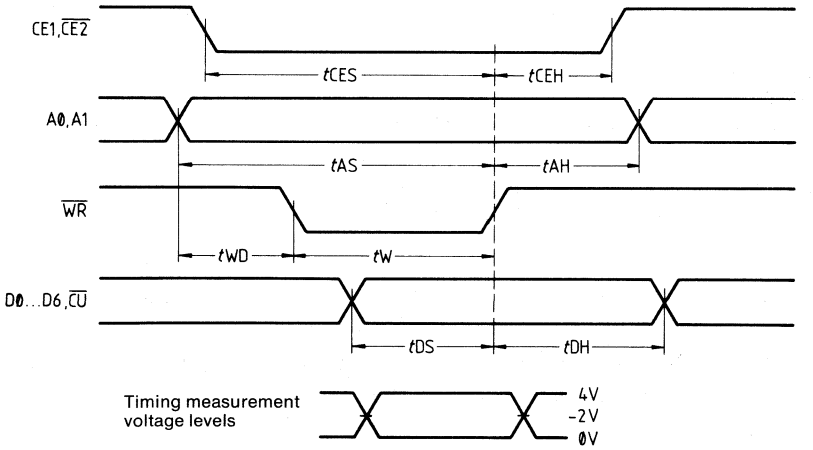
AC characteristics at 25 °C

Timing parameters at V_{CC} = 4.5 V (nanoseconds)

Symbol	Parameter	−20 °C typ.	+25 °C min.	+65 °C typ.
*t*AS	Address setup	300	450	600
*t*WD	Write delay	50	150	175
*t*W	Write pulse	250	300	425
*t*DS	Data setup	150	250	350
*t*DH	Data hold	50	50	100
*t*AH	Address hold	50	50	100
*t*CEH	Chip enable hold	50	50	100
*t*CES	Chip enable setup	300	450	600
*t*CLR	Clear		15 ms	

Timing characteristics

Write cycle waveforms



Loading data

Setting the chip enables (CE1, $\overline{CE2}$) to their true state will enable data loading. The desired data code (DØ...D6) and digit address (AØ, A1) should be held stable during the write cycle for storing new data.

Data entry may be asynchronous and random. (Digit Ø is defined as right hand digit with A1 = AØ = Ø.)

Clearing of the entire internal four-digit memory can be accomplished by holding the clear ($\overline{CLR}$) low for one complete display multiplex cycle, 15 ms minimum.

Loading cursor

Setting the chip enables (CE1, $\overline{CE2}$) and cursor select ($\overline{CU}$) to their true state will enable cursor loading. A write ($\overline{WR}$) pulse will now store or remove a cursor into the digit location addressed by AØ, A1; as defined in data entry. A cursor will be stored if DØ = 1; and will be removed if DØ = Ø. Cursor will **not** be cleared by the $\overline{CLR}$ signal.

For those users not requiring the cursor, the cursor enable signal (CUE) may be tied low to disable display of the cursor function. A flashing cursor can be realized by simply pulsing CUE. If cursor has been loaded to any or all positions in the display, then CUE will control whether the cursor(s) or the characters appear. CUE does not affect the contents of cursor memory.

Display blanking

Blanking the display may be accomplished by loading a blank or space into each digit of the display or by using the ($\overline{BL}$) display blank input.

Setting the ($\overline{BL}$) input low does not affect the contents of either data or cursor memory. A flashing display can be realized by pulsing ($\overline{BL}$).

Notes

1) This display contains a CMOS IC. Normal CMOS handling precautions should be taken to avoid damage due to high static voltages or electric fields.
2) Unused inputs must be tied to an appropriate logic voltage level (either V+ or V−).
3) **Warning** – Do not use solvents containing alcohol!

Loading data state table

Control							Address		Data input							Digit			
$\overline{BL}$	CE1	$\overline{CE2}$	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A1	AØ	D6	D5	D4	D3	D2	D1	DØ	3	2	1	Ø
H	X	X	L	X	H	H	Previously loaded display									G	R	E	Y
H	L	X	L	X	X	H	X	X	X	X	X	X	X	X	X	G	R	E	Y
H	X	X	L	X	X	H	X	X	X	X	X	X	X	X	X	G	R	E	Y
H	X	H	L	X	X	H	X	X	X	X	X	X	X	X	X	G	R	E	Y
H	X	X	L	X	X	H	X	X	X	X	X	X	X	X	X	G	R	E	Y
H	X	X	L	X	H	H	X	X	X	X	X	X	X	X	X	G	R	E	Y
H	H	L	L	H	L	H	L	L	H	L	L	L	H	L	H	G	R	E	E
H	H	L	L	H	L	H	L	H	H	L	H	L	H	L	H	G	R	U	E
H	H	L	L	H	L	H	H	L	H	L	L	H	H	L	L	G	L	U	E
H	H	L	L	H	L	H	H	H	H	L	L	L	L	H	L	B	L	U	E
O	X	X	X	X	H	H	Blank display												
H	H	L	L	H	L	H	H	H	H	L	L	L	H	H	H	G	L	U	E
H	X	X	L	X	X	L	Clears character display									See character set			
H	H	L	L	H	L	H	X	X	See character code										

X = don't care

Loading cursor state table

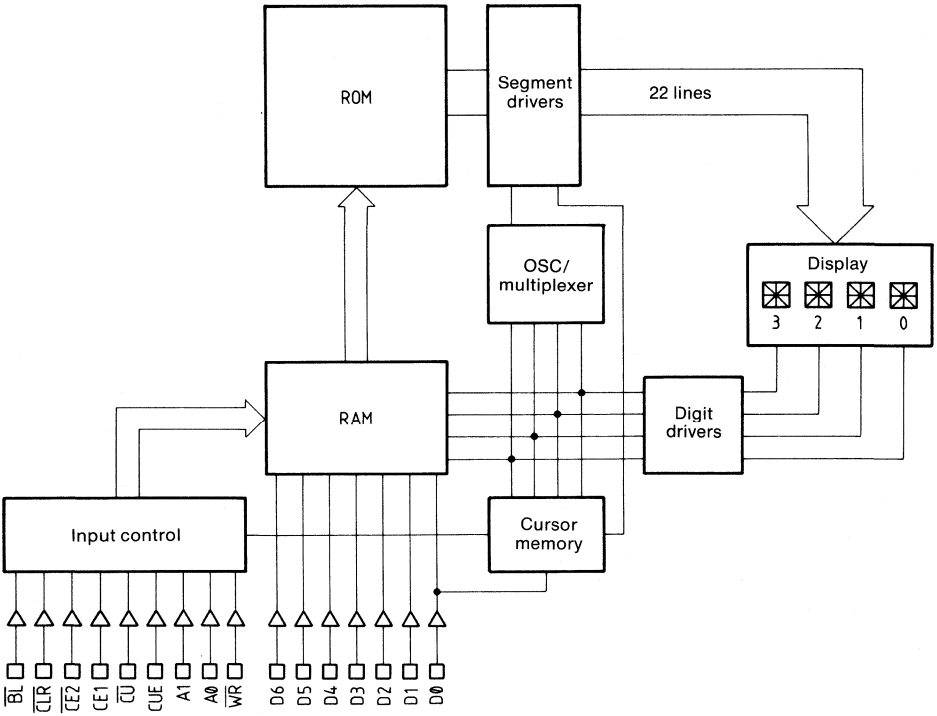
Control							Address		Data input							Digit			
$\overline{BL}$	CE1	$\overline{CE2}$	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A1	AØ	D6	D5	D4	D3	D2	D1	DØ	3	2	1	Ø
H	X	X	L	X	H	H	Previously loaded display									B	E	A	R
H	X	X	H	X	H	H	Display previously stored cursors									B	E	A	R
H	H	L	H	L	L	H	L	L	X	X	X	X	X	X	H	B	E	A	⊠
H	H	L	H	L	L	H	L	H	X	X	X	X	X	X	H	B	E	⊠	⊠
H	H	L	H	L	L	H	H	L	X	X	X	X	X	X	H	B	⊠	⊠	⊠
H	H	L	H	L	L	H	H	H	X	X	X	X	X	X	H	⊠	⊠	⊠	⊠
H	H	L	H	L	L	H	H	L	X	X	X	X	X	X	L	⊠	E	⊠	⊠
H	X	X	L	X	H	H	Disable cursor display									B	E	A	R
H	H	L	L	L	L	H	H	H	X	X	X	X	X	X	L	B	E	A	R
H	X	X	H	X	H	H	Display stored cursors									B	E	⊠	⊠

X ≙ don't care

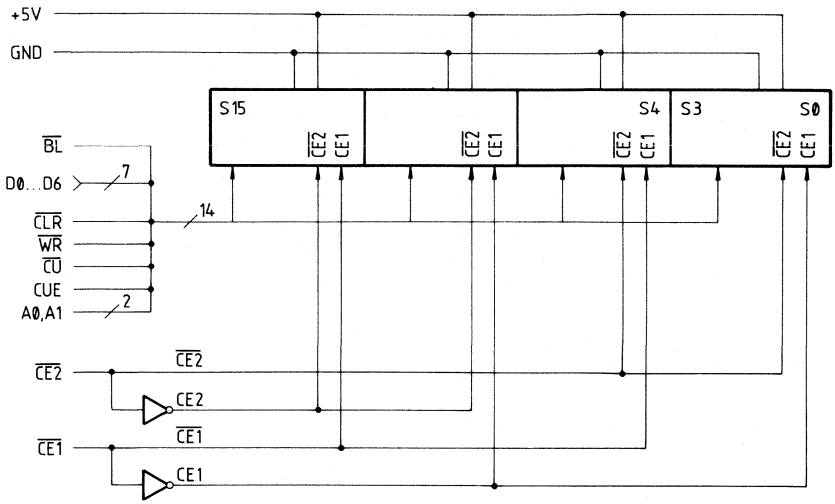
Character set

		D0	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
		D1	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
		D2	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
		D3	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
D6	D5	D4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L	H	L	2		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
L	H	H	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
H	L	L	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
H	L	H	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
H	H	L	6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
H	H	H	7	p	q	r	s	t	u	v	w	x	y	z	{	|	}	~	

Block diagram



Typical schematic for 16-digit system



Alphanumeric intelligent displays with memory, decoder, and driver.

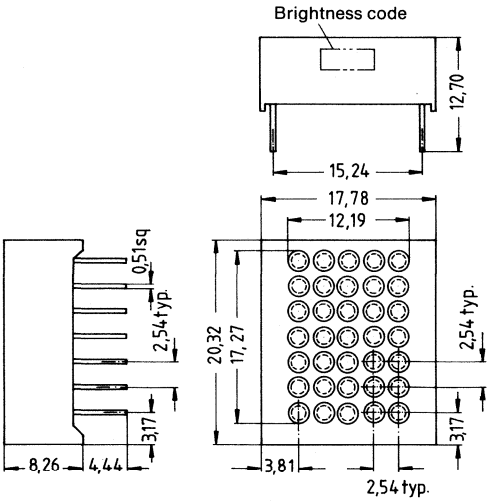
17.3 mm, 5×7 dot matrix

Emission colors: orange, green.

Features

- 17.3 mm high, hybrid character
- Wide viewing angle, ± 75 degrees
- Fully encapsulated, rugged, solid plastic package
- Built-in memory
- Built-in character generator
- Built-in multiplex and LED drive circuitry
- Built-in lamp test
- Intensity control (4 levels)
- 96 character ASCII format
- Microprocessor bus compatible
- Intensity coded for display uniformity
- Single 5 V power supply required
- X/Y stackable

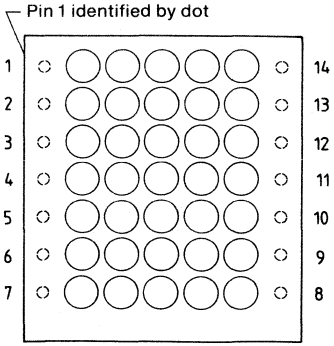
Type	Color	Ordering code
DLO 7135	orange	Q68000–A7157–F114
DLG 7137	green	Q68000–A7159–F114



Dimensions in mm

Pin configuration (top view – display side)

Pin	Function	
1	V_{CC}	Supply voltage
2	$\overline{LT}$	Lamp test
3	$\overline{CE}$	Chip enable
4	$\overline{WR}$	Write
5	$\overline{BL1}$	Brightness
6	$\overline{BLØ}$	Brightness
7	GND	Ground (Ø V)
8	DØ	Data input (LSB)
9	D1	Data input
10	D2	Data input
11	D3	Data input
12	D4	Data input
13	D5	Data input
14	D6	Data input (MSB)



Description

The DLO 7135 and DLG 7137 are single digit, 17.3 mm high 5×7 dot matrix intelligent displays. The built-in CMOS integrated circuit contains memory, ASCII character generator, and LED multiplexing and drive circuitry. Inputs are TTL compatible. A single 5 V power supply is required.

Loading data

Loading data into the DLO 7135 and DLG 7137 is straightforward. Chip enable ($\overline{CE}$) should be present and stable during a write pulse ($\overline{WR}$). Parallel data information should be stable for the minimum time (tDS) and held for tDH after write has gone high. No synchronization is necessary and each character will continue to be displayed until it is replaced with another. Multiple displays may be stacked together with only one additional decoder IC for chip enable decoding.

Lamp test

The lamp test ($\overline{LT}$) when activated causes all dots on the display to be illuminated at half brightness. The lamp test function is independent of write ($\overline{WR}$) and the settings of the blanking inputs ($\overline{BLØ}$; $\overline{BL1}$).

This convenient test gives a visual indication that all dots are functioning properly. Lamp test may also be used as a cursor function or pointer which does not destroy previously displayed characters.

Optoelectronic characteristics at 25 °C

Maximum ratings

Voltage, any pin with respect to GND	−0.5 ... +6.0 V
Operating temperature	−20 ... +65 °C
Storage temperature	−20 ... +70 °C
Relative humidity at 65 °C (non-condensing)	85 %

Optical characteristics (typical)

Luminous intensity/dot (average) at V_{CC} = 5 V:	
DLO 7135	500 µcd
DLG 7137	500 µcd
Digit size	17.27 mm
Viewing angle[1])	±75 degrees
Spectral peak wavelength:	
DLO 7135	630 nm
DLG 7137	565 nm

DC characteristics

Symbol	Parameter	min.	typ.	max.	Test conditions
I_{CC}	V_{CC} supply current (blank)		4.5 mA	8 mA	$\overline{BL0}$ = Ø, $\overline{BL1}$ = Ø, V_{CC} = 5 V
I_{CC}	V_{CC} supply current		160 mA	200 mA	$\overline{BL0}$ = 1, $\overline{BL1}$ = 1, V_{CC} = 5 V
I_{CC}	V_{CC} supply current		80 mA		$\overline{BL0}$ = Ø, $\overline{BL1}$ = 1, V_{CC} = 5 V
I_{CC}	V_{CC} supply current		40 mA		$\overline{BL0}$ = 1, $\overline{BL1}$ = Ø, V_{CC} = 5 V
I_{IL}	Input current – low (any input)			160 µA	V_{IN} = 0.8 V, V_{CC} = 5 V
V_{IL}	Input voltage – low (any input)			1.0 V	V_{CC} = 5 V
V_{IH}	Input voltage – high (any input)	3.0 V			V_{CC} = 5 V

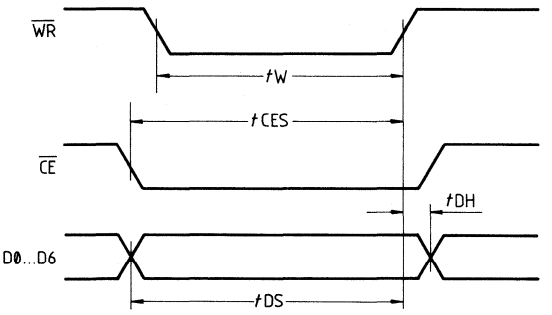
[1]) "Off Axis Viewing Angle" is here defined as: "the minimum angle in any direction from the normal to the display surface at which any part of any dot in the display is not visible".

AC characteristics

Minimum timing parameters at V_{CC} = 4.5 V (nanoseconds)

Symbol	Parameter	−20 °C	+25 °C	+65 °C	Unit
*t*CES	Chip enable setup	130	200	270	ns
*t*DS	Data setup	130	200	270	ns
*t*W	Write pulse	130	200	270	ns
*t*DH	Data hold	65	100	135	ns

Timing characteristics



Notes

1) This display contains a CMOS integrated circuit. Normal CMOS handling precautions should be taken to avoid damage due to high static voltages or electric fields.
2) Unused inputs must be tied to an appropriate logic voltage level (either V+ or V−).
3) V_{CC} = 5.0 V ±10 %.
4) Clean only in water, isopropyl alcohol, freon TF or TE (or equivalent).

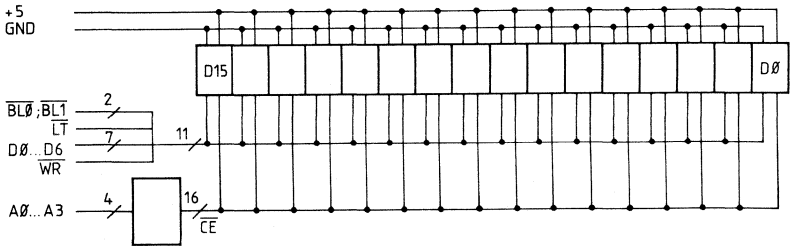
Dimming and blanking the display

Brightness level	$\overline{BL1}$	$\overline{BL\emptyset}$
Blank	Ø	Ø
¼ brightness	Ø	1
½ brightness	1	Ø
Full brightness	1	1

Data loading example

$\overline{CE}$	$\overline{WR}$	$\overline{BL\emptyset}$	$\overline{BL1}$	$\overline{LT}$	Data input D6	D5	D4	D3	D2	D1	DØ	
H	X	H	X	H	X	X	X	X	X	X	X	NC
X	X	L	L	H	X	X	X	X	X	X	X	Blank
X	X	X	X	L	X	X	X	X	X	X	X	Lamp test
L	L	X	H	H	H	L	L	L	L	L	H	A
L	L	H	H	H	H	H	H	L	L	H	L	r
L	L	H	H	H	L	H	H	L	L	H	H	3
L	L	H	H	H	L	H	L	H	L	H	H	+

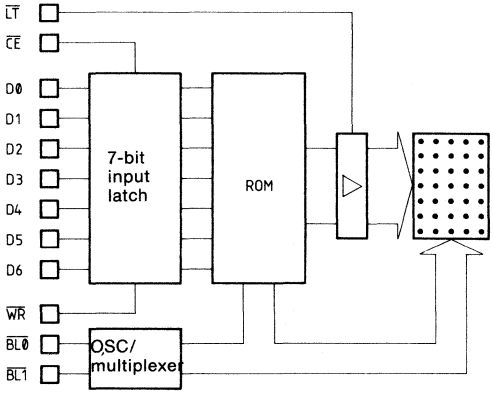
16 character interconnection



Character set

			D0	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
			D1	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
			D2	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
			D3	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
D6	D5	D4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
L	L	L	0	Blanked characters															
L	L	H	1																
L	H	L	2		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
L	H	H	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
H	L	L	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
H	L	H	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
H	H	L	6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
H	H	H	7	p	q	r	s	t	u	v	w	x	y	z	{	|	}	~	

Block diagram



D0...D6	Data inputs
WR	Write
CE	Chip enable
BL0, BL1	Brightness level
LT	Lamp test

Application Notes
5×7 Dot Matrix Intelligent Displays
DLO 7135, DLG 7137

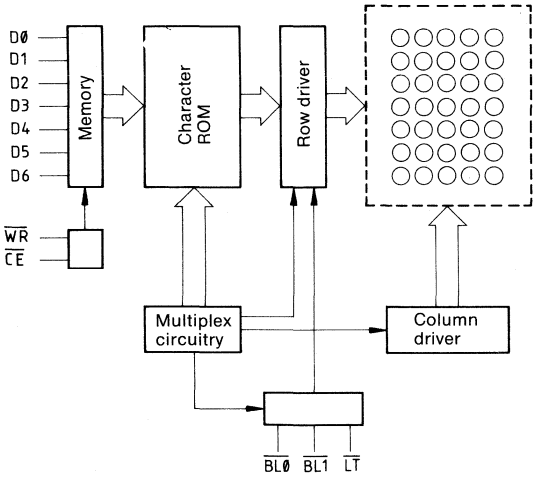
This application note is intended to serve as a design and application guide for users of the DLO 7135 and DLG 7137 intelligent displays. The information presented covers device electrical description, operation, general circuit design considerations, and interfacing with microprocessors.

Electrical description

If you have never designed a system using a dot matrix display before, you cannot appreciate the simplicity of using the DLX 713*[1]) intelligent alphanumeric 5×7 dot matrix display. The intelligent display contains memory, character generator, multiplexing circuits, and drivers built into a single package.

Figure 1 is a block diagram of the DLX 713*. The unit consists of 35 LED die arranged in a 5×7 pattern and a single CMOS integrated circuit chip. The IC chip contains the segment drivers, digit drivers, 96 character generator ROM, memory, multiplex and blanking circuitry.

Figure 1
Block diagram

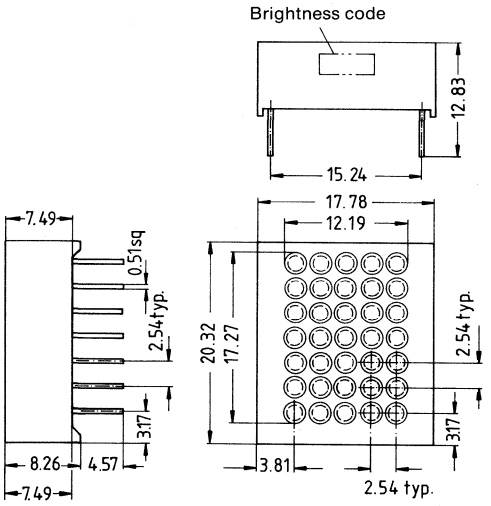


[1]) DLX 713* means:
DLO 7135, DLG 7137.

Package

The 35 dots form a 12.2×17.3 mm overall character size in a 17.8×20.3 mm dual-in-line package. The ±75 degree wide viewing angle complements the large display and is the ideal display for industrial control applications. Display construction is a filled reflector type with the integrated circuit in the back and then filled with IC-grade epoxy. This results in a very rugged part which is quite impervious to moisture, shock, and vibration.

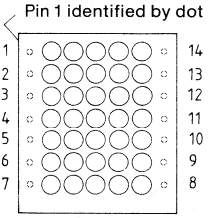
Figure 2



Dimensions in mm

Pin configuration (top view – display side)

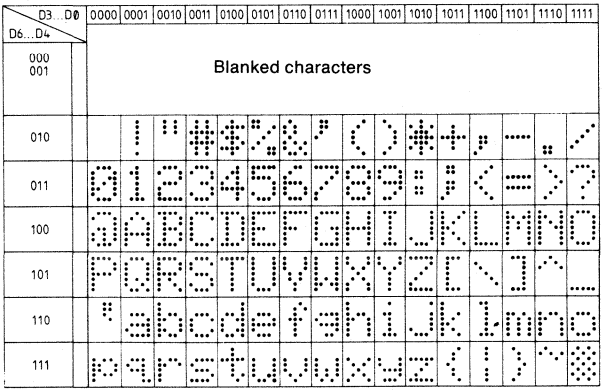
Pin	Function	
1	V_{CC}	Supply voltage (+5 V)
2	$\overline{LT}$	Lamp test
3	$\overline{CE}$	Chip enable
4	$\overline{WR}$	Write
5	$\overline{BL1}$	Brightness
6	$\overline{BL\emptyset}$	Brightness
7	GND	Ground (Ø V)
8	DØ	Data input (LSB)
9	D1	Data input
10	D2	Data input
11	D3	Data input
12	D4	Data input
13	D5	Data input
14	D6	Data input (MSB)



Electrical inputs

V_{CC}	Positive supply voltage +5 V
GND	Ground
DØ...D6	Data lines (see **figure 3** for character set)
$\overline{CE}$	Chip enable (active low) This determines which device in an array will accept data
$\overline{LT}$	Lamp test (active low) Causes all dots to light at ½ brightness
$\overline{WR}$	Write (active low) Data and chip enable must be present and stable before and after the write pulse (see page 107 for timing)
$\overline{BLØ}$, $\overline{BL1}$	Blanking control input (active low) Used to control the level of display brightness

Figure 3
Character set



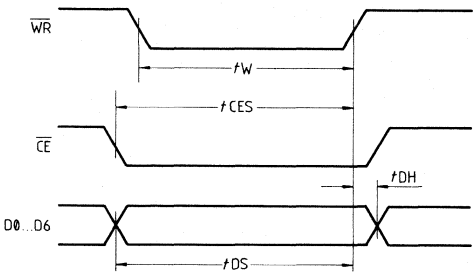
Operation

In a dot matrix display system, it is advantageous to use a multiplexed approach with 12 drivers (5 digits + 7 segments) rather than 35 segment drivers. This obviously reduces the number of drivers and interconnections required. A multiplexed system must be a synchronous system or the digits or elements may have different on (lit) times and therefore varying brightness.

The DLX 713* is an internally multiplexed display but the data entry is asynchronous. Loading data is similar to writing into a RAM. Present the data, select the chip, and give a write signal. For a multidigit system, each digit has its own unique location and will display its contents until replaced by another code.

The waveforms of **figure 4** demonstrate the relationship of the signals required to generate a write cycle. Check the data sheet on page 107 for minimum values required for each signal.

Figure 4
Timing characteristics



Display blanking and dimming

The DLX 713* intelligent display has the capability of three levels of brightness plus blank. **Figure 5** shows the combination of $\overline{BL0}$ and $\overline{BL1}$ for the different levels of brightness. The $\overline{BL0}$ and $\overline{BL1}$ inputs are independent of write and chip enable and do not affect the contents of the internal memory. A flashing display can be achieved by pulsing the blanking pins at a 1...2 Hz rate.

Figure 5
Blanking and dimming control

Brightness level	$\overline{BL1}$	$\overline{BL0}$
Blank	0	0
¼ brightness	0	1
½ brightness	1	0
Full brightness	1	1

Lamp test

The lamp test ($\overline{LT}$) when activated causes all dots on the display to be illuminated at half brightness. It does not destroy any previously stored characters. The lamp test function is independent of chip enable ($\overline{CE}$), write ($\overline{WR}$), and the settings of the blanking inputs $\overline{BL1}$ and $\overline{BL0}$.

This convenient test gives a visual indication that all dots are functioning properly. Because of the lamp test not affecting the display memory, it can be used as a cursor or pointer in a line of displays.

General design considerations

When using the DLX 713* on a separate display board having more than 15 cm of cable length, it may be necessary to buffer all of the input lines. A non-inverting 74365 hex buffer can be used. The object is to prevent transient current into the DLX713* protection diodes. The buffers should be located of the display board and as close to the displays as possible.

Because of high switching currents caused by the multiplexing, local power supply by-pass capacitors are also needed in many cases. These should be 6 V or 10 V, tantalum type having 5 µF · 10 µF capacitance. The capacitors may only be required every 6...7 displays depending on the line regulation and other noise generators.

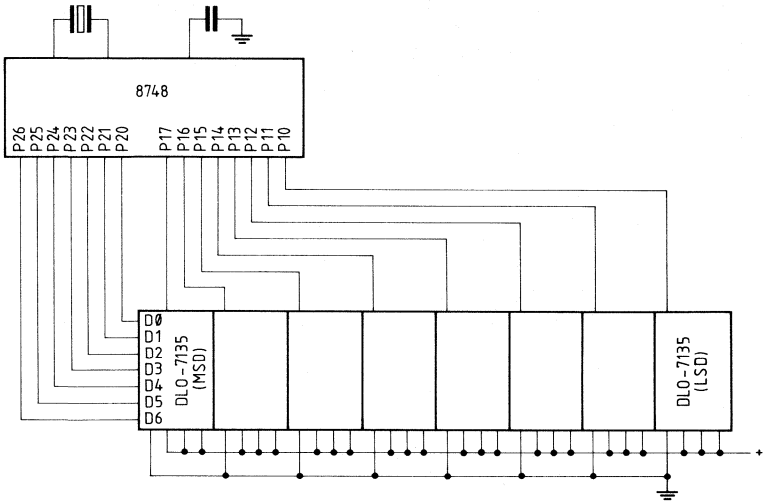
If small wire cables are used, it is good engineering practice to calculate the wire resistance of the ground and the + 5 V wires. More than 0.2 V drop (at 100 mA per digit) should be avoided, since this loss is in addition to any inaccuracies or load regulation of the power supply.

The 5 V power supply for the DLX 713* should be the same one supplying the V_{CC} to all logic devices. If a separate supply must be used, then local buffers should be used on all the inputs and these buffers should be powered from the display power supply. This precaution is to avoid line transients or any logic signals to be higher than V_{CC} during power up.

Interfacing

For an eight digit display using the DLX 713*, interfacing to a single chip microprocessor such as the 8748 is easy and straightforward. One approach may be to dedicate one port for the six data signals and another 8-bit port for the write signals. The schematic is shown in **figure 6**.

Figure 6
DLO 7135 interface with 8748

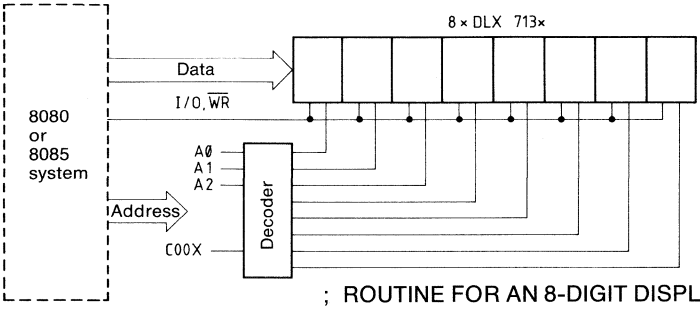



```
                        ; SUBROUTINE TO LOAD AN 8-DIGIT
                        ; DISPLAY USING THE DL7135
                        ; DATA IN RAM 10H-17H (MSD-LSD)
INIT:   ORL   P1, #OFFH ; PORT 1 ALL HIGH (WRITE)
        ORL   P2, #ØØH  ; PORT 2 ALL LOW (DATA)
        MOV   R1, #OFH  ; RAM ADDRESS – 1
        MOV   R2, #ØFEH ; WRITE PULSE
        MOV   R3, #Ø8H  ; COUNTER
START:  INC   R1        ; INCREMENT RAM POINTER
DATA:   MOV   A, @R1    ; FETCH DATA FROM RAM
        OUTL  P2,A      ; LOAD PORT 2
        MOV   A,R2      ; RECALL WRITE
        RR    A         ; SHIFT A TO NEXT WRITE
        MOV   R2,A      ; SAVE WRITE
WRITE:  OUTL  P1,A      ; SEND WRITE PULSE
        MOV   A, #ØFFH  ; WAIT
        OUTL  P1,A      ; RESET WRITE PULSE
        DJNZ  R3, START ; LOAD COMPLETE?
        RET             ; RETURN TO MAIN PROGRAM
```

I/O or memory-mapped system

For a memory-mapped system using a processor such as the 8080 or 8085, the interfacing is also straightforward. Each display is treated as a memory location with its own address, like another I/O or RAM location.

Figure 7
Block diagram for 8-digit DLX 713* dot-matrix display




```
                        ; ROUTINE FOR AN 8-DIGIT DISPLAY
                        ; USING THE DLX 713* AND
                        ; 8085 OR 8080 MICROPROCESSOR
                        ;
                        ; DATA TO BE DISPLAYED IS IN
                        ; AØ(LSD) THRU A8(MSD)
                        ;
                        ; DISPLAY ADDRESS C00X
                        ; LSD IS RIGHT MOST DIGIT
                        ;
                        ; DOES NOT SAVE REG A,B,H,L,D,E
                        ;
DADD:   EQU   ØAØØØH    ; DATA ADDRESS LOCATION
DPAD:   EQU   ØCØØØH    ; DISPLAY ADDRESS LOCATION
LEN:    EQU   Ø8H       ; DISPLAY LENGTH
                        ;
ORG:    100H
                        ;
DISP:   LXI   H,DADD    ; LOAD DATA ADDRESS
        LXI   D,DPAD    ; LOAD DISPLAY ADDRESS
        MVI   B,LEN     ; LOAD DISPLAY LENGTH
DISP1:  MOV   A,M       ; GET DATA
        XCHG            ; XCHG H/L & D/E
        MOV   M,A       ; LOAD DISPLAY FROM REG A
        XCHG            ; RESTORE H/L & D/E
        INX   D         ; INCREMENT DISPLAY ADDRESS
        INX   H         ; INCREMENT DATA ADDRESS
        DCR   B         ; DECREMENT LENGTH COUNTER
        JNZ   DISP1     ; END OF DISPLAY?
        RET             ; RETURN TO MAIN PROGRAM
```

The interface schemes shown demonstrate the simplicity of using the DLX 713* dot matrix intelligent display. Slight timing differences may be encountered for various microprocessors, but can be resolved similar to those encountered when using different RAMs. The techniques used in the examples were shown for their generality. The user will undoubtedly invent other schemes to optimize his particular system to its requirements.

Note

Note that although other manufacturer's products are used in the examples, this application note does not imply specific endorsement, or warranty of other manufacturer's products by Siemens.

Intelligent Display Assemblies

Intelligent display assemblies are preassembled display systems. They consist of intelligent displays, address decoding circuitry, an input buffering circuit, and power decoupling capacitors in a pretested, compact module. These microprocessor display peripheral systems offer the following benefits:

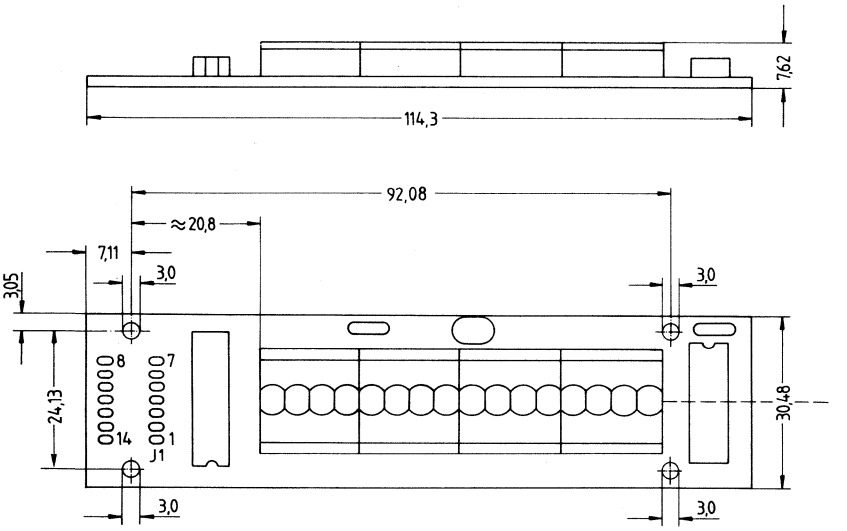
- Minimized design time for faster product introduction
- Cost-effective pricing for moderate quantity production runs
- Ideal suitability for system development and upgrading of existing designs
- Easy interfacing through commercially available connectors

Alphanumeric intelligent display assembly with memory, decoder, and driver.
2.8 mm, red, 16 digits, 17 segments.

Features

- 2.8 mm high, magnified monolithic characters
- Wide viewing angle ±40 degrees
- Complete alphanumeric display assembly utilizing the DL 1414
  - built-in multiplex and LED drive circuitry
  - built-in memory
  - built-in character generator
- Displays 64 character ASCII set
- Direct access to each digit independently
- Single 5 V power supply
- TTL-compatible
- Easily interfaced with a microprocessor
- IDA 1414–16–1: Input data lines buffered
  IDA 1414–16–2: Input data lines not buffered

Type	Ordering code
IDA 1414–16–1	Q68000–A6380–F114 (buffered)
IDA 1414–16–2	Q68000–A6381–F114 (non-buffered)



Dimensions in mm

Pin configuration

Pin	Function		Pin	Function	
1	AØ	Digit select	14	V_{CC}	Supply voltage (+5 V)
2	A1	Digit select	13	D5	Data input
3	D4	Data input	12	D1	Data input
4	DØ	Data input (LSB)	11	D6	Data input (MSB)
5	D3	Data input	10	A2	Digit select
6	D2	Data input	9	$\overline{WR}$	Write
7	GND	Ground	8	A3	Digit select

Wires may be soldered directly to a 14 hole, dual-in-line pattern, or contact can be made with ribbon cables and connectors, such as:

Siemens C42334–A368–A15	Berg 65493–006
Siemens C42334–A368–A14	AMP 86838–1
Siemens C42334–A390–A14	AMP 86838–2

Description

The IDA 1414–16 assembly is an extension of the very easy-to-use DL1414 intelligent display. This product provides the designer with circuitry for display maintenance. It also minimizes interaction and interface normally required between the user's system and a multiplexed alphanumeric display.

The assembly consists of four DL 1414s in a single trow, together with decoder and interface buffers on a single printed circuit board. Each DL1414 provides its own memory, ASCII ROM character decoder, multiplexing circuitry, and drivers for its four 17-segment LEDs.

Intelligent display assemblies can be used for applications such as data terminals, controllers, instruments, and other products which require an easy-to-use alphanumeric display.

Optoelectronic characteristics at 25 °C

Maximum ratings

Supply voltage	6.0 V
Voltage at any input	$-0.5 \ldots V_{CC} + 0.5$ V
Operating temperature	0 ... +65 °C
Storage temperature	−20 ... +70 °C
Relative humidity at 65 °C (non-condensing)	85 %

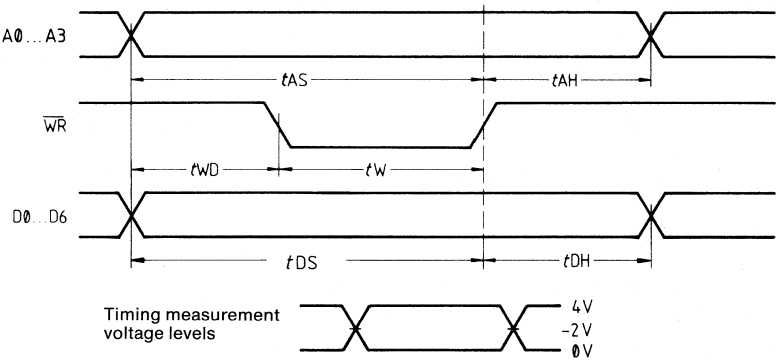
DC characteristics

Symbol	Parameter	min.	typ.	max.	Unit	Test conditions
V_{CC}	Supply current	4.75		5.25	V	
I_{CC}	V_{CC} supply current (total) IDA 1414–16–1: IDA 1414–16–2:			 400 380	 mA mA	V_{CC} = 5.0 V (10 segments/digit)
I_{CC}, blank	V_{CC} supply current (display blank) IDA 1414–16–1: IDA 1414–16–2:			 75 25	 mA mA	V_{CC} = 5.0 V V_{IN} = 0 V
V_{IH}	Input voltage – high –1: (DØ...D6, A2, A3, $\overline{WR}$)	2.0			V	
	–1: (AØ, A1)	2.7			V	V_{CC} = 4.5 V
		3.5			V	V_{CC} = 5.5 V
	–2: (DØ...D6, AØ, A1)	2.7			V	V_{CC} = 4.5 V
		3.5			V	V_{CC} = 5.5 V
	–2: (A2, A3, $\overline{WR}$)	2.0			V	
V_{IL}	Input voltage – low (all inputs)			0.8	V	V_{CC} = 4.5 V
I_{IH}	Input current – high (all inputs)			20	µA	V_{CC} = 5.5 V V_{IH} = 2.7 V
I_{IL}	Input current – low (all inputs)			640	µA	V_{CC} = 5.5 V V_{IL} = 0.4 V
I_V	Luminous intensity (average per digit)		0.5		mcd	V_{CC} = 5.0 V (8 segments/digit)
λ_{peak}	Peak emission wavelength		660		nm	—
	Viewing angle		±40		degrees	

Switching characteristics at 5 V and 25 °C (nanoseconds)

Symbol	Parameter	+25 °C min.	Unit
*t*AS	Address setup	575	
*t*WD	Write delay	150	
*t*W	Write pulse	425	ns
*t*DS	Data setup	575	
*t*DH	Data hold	150	
*t*AH	Address hold	150	

Timing characteristics
Write cycle waveforms



Character set

	D6	D5	D4	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
D0					L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
D1					L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
D2					L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
D3					L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
	L	H	L	2		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
	L	H	H	3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
	H	L	L	4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
	H	L	H	5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_

System overview

The intelligent display assembly offers the designer 16 alphanumeric characters and operates from just a 5 V supply. Based on the previously introduced DL1414 four character intelligent display, the IDA 1414–16 adds all the support logic required for direct connection to most microprocessor buses. The system interface takes place through a 14 hole dual-in-line pattern. The user may solder wires directly into these holes or use a ribbon cable and connectors.

System power requirements

Operating from a single +5 V power supply, the IDA 1414–16 requires a maximum operating current of 400 mA with ten of the segments lit on each character. With the display blanked, the board circuitry draws 75 mA maximum.

Display interface

The display interface available on the 14-pin, dual-in-line hole pattern consists of seven data lines (DØ to D6), four address lines (AØ to A3), write pulse, V_{CC}, and GND.

$\overline{WR}$ (Write, active low): to store a character in the display memory, this line must be pulsed low for a minimum of 425 ns. See timing diagram for timing and relationships to other signals.

Address lines AØ to A3 are set up so that the right-most character is the lowest address. The left-most character is the highest address. Data lines are set up so that DØ is the least significant bit and D6 is the most significant bit.

Using the display interface

Through the use of memory-mapped I/O techniques, the IDA can be treated almost like a memory location – supply the data, address and proper control signals and the characters appear, with each character location independently addressable. The basic signal flow sequence to load a character would start with the address lines going to the desired address. After the address has stabilized, the data can change to the desired values. After the data has stabilized, the $\overline{WR}$ pulse is started, and must remain low for at least 425 ns. Signals must be held stable for 150 ns, minimum, after the rising edge of the $\overline{WR}$ pulse to ensure correct loading, while the addresses must be stable for 575 ns preceding the same rising edge of the $\overline{WR}$ pulse. See the timing diagram for a pictorial explanation.

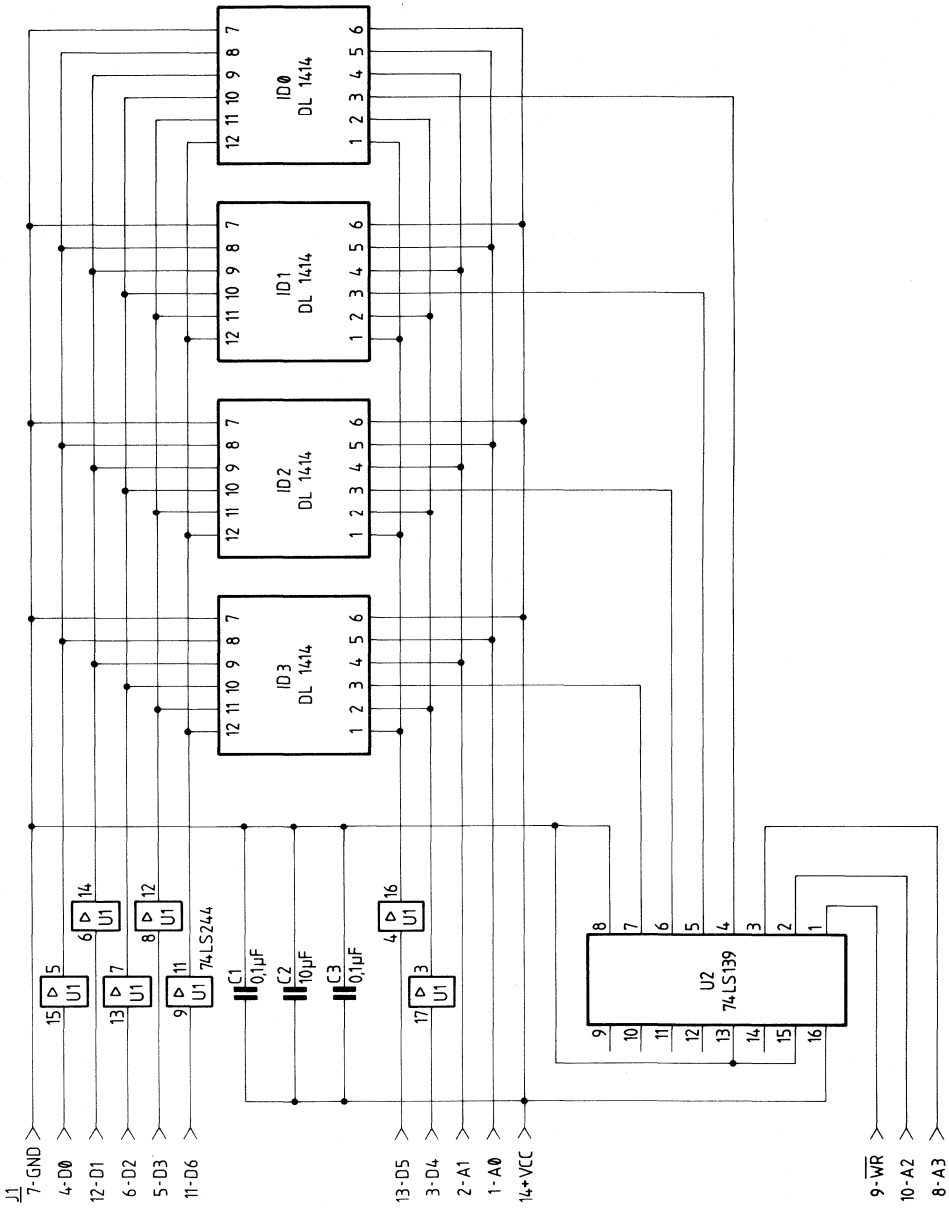
System design considerations

It is often necessary, because of the nature of displays, to use ribbon cables from the CPU board. We have provided a 14 pin dual-in-line hole pattern for this purpose. In those circumstances for cables over 15 cm, use IDA 1414–16–1 (buffered version) instead of IDA 1414–16–2 (non-buffered version). Voltage transients from noisy systems may couple through the cables into the intelligent display and can cause serious damage.

Avoid handling the assembly other than by the edges of the PCB. Static damage can still be a problem, so take the necessary precautions. Keep in conductive material, grounded work areas, etc.

The IDA 1414–16 assemblies should need minimal cleaning. A gentle wiping with a soft damp cloth should be its only requirement. The solvent that cannot be used on any intelligent display product is alcohol. Therefore, if a solvent is used, first check chemical composition before application.

Internal block diagram

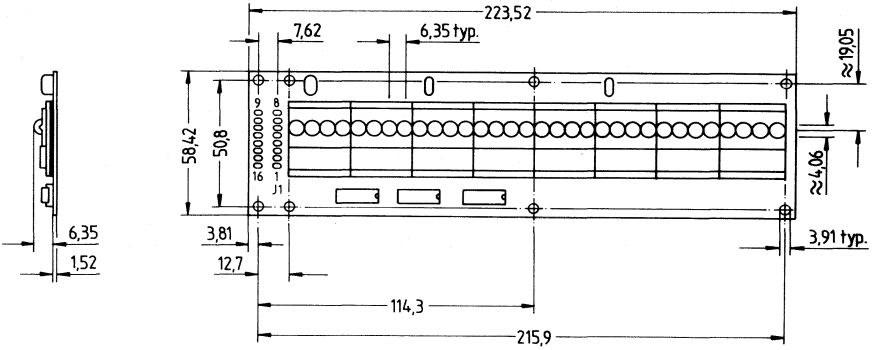


Alphanumeric intelligent display assembly with memory, decoder, and driver.
4.1 mm, red, 32 digits, 16 segments

Features

- 4.1 mm high, magnified monolithic characters
- Complete alphanumeric display assembly utilizing the DL 1416
  - built-in multiplex and LED drive circuitry
  - built-in memory
  - built-in character generator
- Displays 64 character ASCII set
- Direct access to each digit independently
- All inputs buffered
- Cursor function
- Single 5 V power supply
- Easily interfaced to a microprocessor

Type	Ordering code
IDA 1416–32	Q68000–A6382–F114



Dimensions in mm

Pin configuration

Pin	Function	Pin	Function
1	D1 Data input	16	V_{CC} Supply voltage (+5 V)
2	A1 Digit select	15	DØ Data input
3	D6 Data input	14	$\overline{WR}$ Write
4	AØ Digit select	13	D3 Data input
5	D4 Data input	12	$\overline{CU}$ Cursor input
6	D2 Data input	11	D5 Data input
7	A3 Digit select	10	A4 Digit select
8	GND Ground (0 V)	9	A2 Digit select

Wires may be soldered directly to a 16 hole dual-in-line pattern, or contact can be made with ribbon cables and connectors, such as

Siemens C42334–A368–A17
Siemens C42334–A368–A16
Siemens C42334–A390–A16

Berg 65493–008
AMP 86839–1
AMP 86839–2

Description

The IDA 1416–32 assembly is an extension of the very easy-to-use DL 1416 intelligent display. This product provides the designer with circuitry for display maintenance. It also minimizes interaction and interface normally required between the user's system and a multiplexed alphanumeric display.

The assembly consists of eight DL 1416s in a single row together with decoder and interface buffers on a single printed circuit board. Each DL 1416 provides its own memory, ASCII ROM character decoder, multiplexing circuitry, and drivers for its four 16-segment LEDs.

Intelligent display assemblies can be used for applications such as data terminals, controllers, instruments, and other products which require an easy-to-use alphanumeric display.

Optoelectronic characteristics at 25 °C

Maximum ratings

Supply voltage	6.0 V
Voltage at any input	$-0.5 \ldots V_{CC} + 0.5$ V
Operating temperature	0 ... +65 °C
Storage temperature	−20 ... +70 °C
Relative humidity at 65 °C (non-condensing)	85 %

DC characteristics

Symbol	Parameter	min.	typ.	max.	Unit	Test conditions
V_{CC}	Supply voltage	4.75		5.25	V	
I_{CC}, Cursor	V_{CC} supply current[1] Cursor			1250	mA	V_{CC} = 5.0 V (all segments on)
I_{CC}, blank	V_{CC} supply current (blank) total			100	mA	V_{CC} = 5.0 V inputs low
I_{CC}	V_{CC} supply current		390		mA	V_{CC} = 5.0 V (10 segments/digit)
V_{IH}	Input voltage – high	2			V	V_{CC} = 5.0 V
V_{IL}	Input voltage – low			0.8	V	V_{CC} = 5.0 V
I_{IH}	Input current – high			40	µA	V_{CC} = 5.25 V V_{IH} = 2.4 V
I_{IL}	Input current – low			−1.6	mA	V_{CC} = 5.25 V V_{IL} = 0.4 V
I_V	Luminous intensity (average per digit)		0.5		mcd	V_{CC} = 5.0 V (8 segments/digit)
λ_{peak}	Peak emission wavelength		660		nm	—
	Viewing angle		±20		degrees	

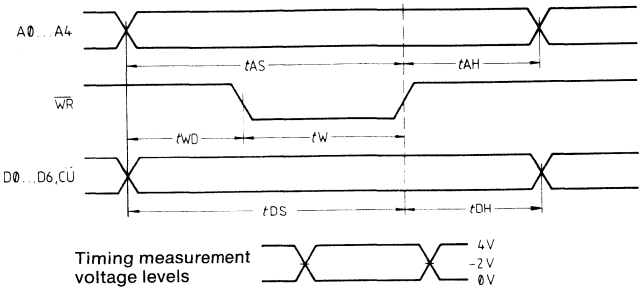
[1]) Max. duration: 60 s

Switching characteristics at 5 V and 25 °C (nanoseconds)

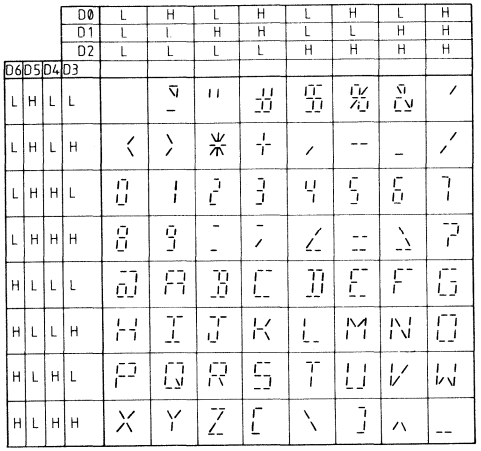
Symbol	Parameter	+25 °C min.	Unit
*t*AS	Address setup	1300	
*t*WD	Write delay	650	
*t*W	Write pulse	650	ns
*t*DS	Data setup	1300	
*t*DH	Data hold	550	
*t*AH	Address hold	550	

Timing characteristics

Write cycle waveforms



Character set



All undefined data codes that are loaded or occur on power-up will cause a blank display state.

System overview

The IDA 1416–32 intelligent display assembly offers the designer 32 alphanumeric characters and operates from just a +5 A supply. Based on the previously introduced DL 1416 four character intelligent display, the IDA 1416–32 adds all the support logic required for direct connection to a host system.

System power requirements

Operating from a single +5 V power supply, the IDA 1416–32 requires a typical operating current of 390 mA with ten segments lit for each digit. The maximum operating current with all segments lit for all digits will be 1250 mA maximum.

Display interface signals

The system interface takes place through a 16 hold dual-in-line pattern. The user may solder wires directly into these holes or use a ribbon cable connector. The interface signals available at the 16 holes consist of seven data lines (DØ to D6), five address lines (AØ to A4), write and cursor input.

$\overline{WR}$ (Write, active low): to store a character in the display memory must meet minimum write cycle waveform.

$\overline{CU}$ (Cursor select, active low): this input must be held high during a write cycle to load ASCII data into memory; and held low during a write cycle to load cursor data into memory. The cursor ($\overline{CU}$) should not be hardwired high (off). During the power-up of the DL 1416s the cursor memory will be in a random state. Therefore, it is recommended for the host system to initialize or write out all possible cursors during system initialization. Also, the cursor display will be overridden by a blank from an undefined code in that digit position.

Address lines AØ to A4 are set up so that the right-most character is the lowest address location. The left-most character is the highest address. Data lines are set up so that DØ is the least significant bit and D6 the most significant bit.

Using the display assembly

Through the use of memory-marked I/O techniques, the IDA can be treated almost like a memory location – supply the data, address, proper control signals and the characters appear, with each character location independently addressable. The basic signal flow sequence to load a character would start with the address lines going to the desired address. Data can change to the desired values (including cursor). After the data has stabilized, the write ($\overline{WR}$) pulse is started. See specifications and timing diagram for times and pictorial explanation.

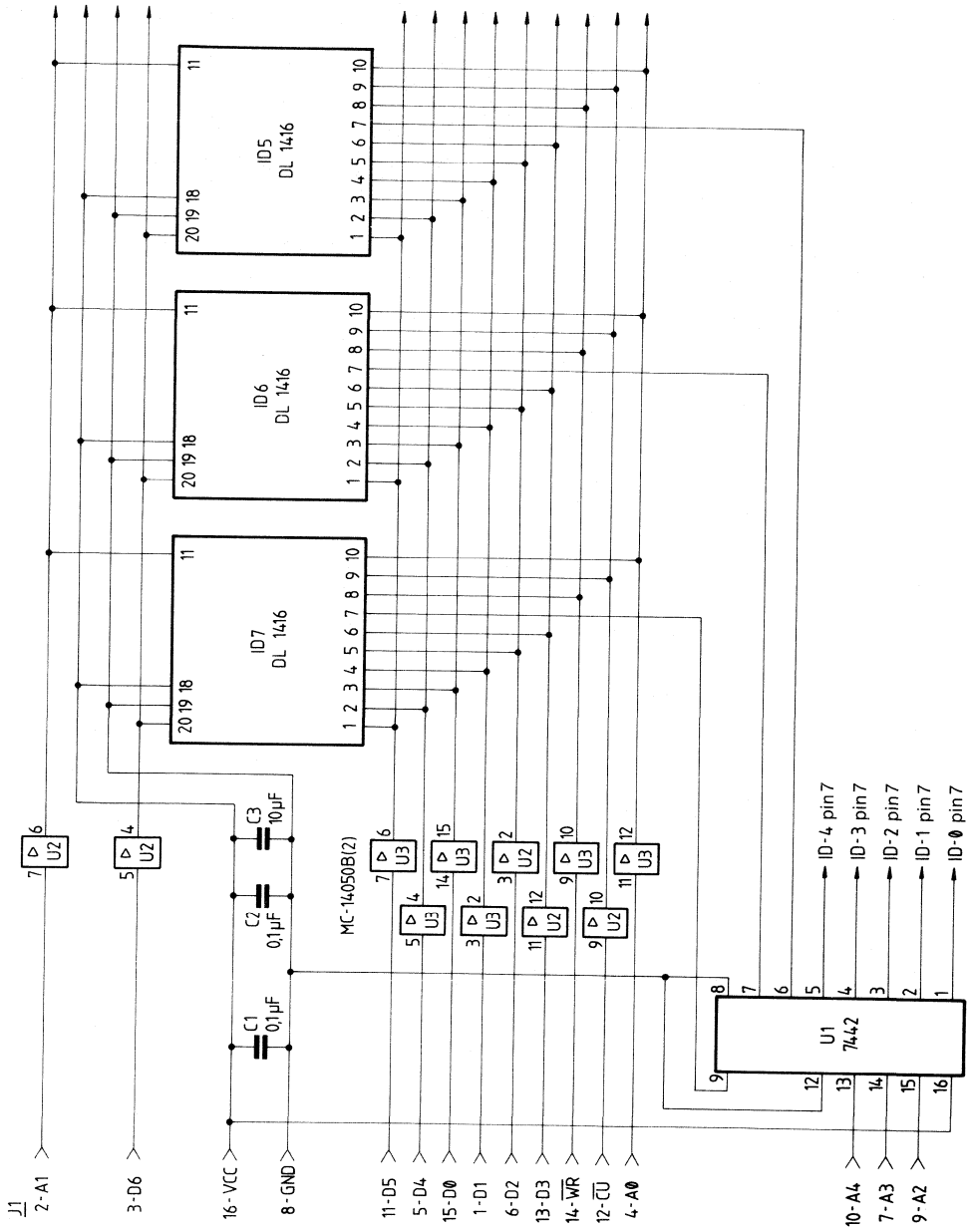
System design considerations

It is often necessary, because of the nature of displays, to use cables. Avoid excessively long cables; try to keep them short. Because of current steps due to internal multiplexing, wire length and size will affect load regulation which may cause an incorrect display.

Avoid handling the assembly other than by the edges of the PCB. Static damage can still be a problem, so take the necessary precautions. Keep in conductive material, grounded work areas, etc.

The IDA 1416–32 requires minimal cleaning. A gentle wiping with a soft damp cloth should be its only requirement. The solvent that cannot be used on any intelligent display product is alcohol. Therefore, if a solvent is used, first check chemical composition before application.

Block diagram

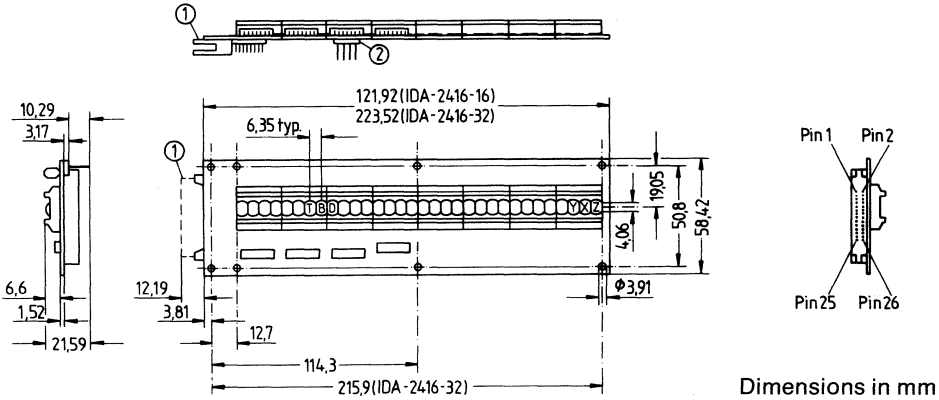


Alphanumeric intelligent display assembly with memory, decoder, and driver.
4.1 mm, red, 16 or 32 digits, 16 segments plus decimal.

Features

- Complete alphanumeric display assembly utilizing the DL 2416
  - built-in multiplex and LED drive circuitry
  - built-in memory
  - built-in character generator
- Displays 64 character ASCII set
- Direct access to each digit independently
- Display blank function
- Memory clear function
- Cursor function
- Choice of 16 or 32 character display length (other lengths optional)
- Single 5 V power supply
- TTL-compatible
- Easily interfaced to a microprocessor
- Tristate or open-collector input circuitry
- Schmitt Trigger inputs on control lines

Type	Ordering code
IDA 2416–16	Q68000–A6375–F114
IDA 2416–32	Q68000–A6376–F114



Dimensions in mm

Recommended mating connector

Connector	Function	Type	Suggested mfg.
① J2	Control/data	26 pin ribbon	BERG P/N 65480–011
② J3	Power	Molex	AMP P/N 1–87025–3

Pin configuration

Pin	Function		Pin	Function	
J2–1	A2	Address line	J2–14		No connection
J2–2	$\overline{DE4}$	Display enable	J2–15	D6	Data line
J2–3	A3	Address line	J2–16		No connection
J2–4	$\overline{DE3}$	Display enable	J2–17	D4	Data line
J2–5	A4	Address line	J2–18	CUE	Cursor enable
J2–6	$\overline{DE1}$	Display enable	J2–19	D5	Data line
J2–7		No connection	J2–20	$\overline{CU}$	Cursor select
J2–8	$\overline{DE2}$	Display enable	J2–21	AØ	Address line
J2–9	DØ	Data line	J2–22	$\overline{CLR}$	Clear
J2–10		No connection	J2–23	A1	Address line
J2–11	D1	Data line	J2–24	$\overline{WR}$	Write
J2–12		No connection	J2–25	D3	Data line
J2–13	D2	Data line	J2–26	$\overline{BL}$	Blanking
J3–1	GND	Ground	J3–3	V_{CC}	Supply voltage (+5 V)
J3–2	V_{CC}	Supply voltage (+5 V)	J3–4	GND	Ground

The IDA 2416 series assembly is an extension of the very easy-to-use DL 2416 intelligent display. This product provides the designer with circuitry for display maintenance. It also minimizes interaction and interface normally required between the user's system and a multiplexed alphanumeric display.

The assembly consists of DL 2416s in a single row together with decoder and interface buffers on a single printed circuit board. Each DL 2416 provides its own memory, ASCII ROM character decoder, multiplexing circuitry, and drivers for its four 17-segment LEDs.

Intelligent display assemblies can be used for applications such as data terminals, controllers, instruments, and other products which require an easy-to-use alphanumeric display.

Type	Description
IDA 2416–16	Single line, 16 character alphanumeric display utilizing 4 displays of DL 2416
IDA 2416–32	Single line, 32 character alphanumeric display utilizing 8 displays of DL 2416
IDA 2416–XX–YY	Single line alphanumeric display utilizing the DL 2416 display XX – indicates number of characters (groups of four) from 16 to 40 YY – options or special versions
	Detailed information upon request

System overview

The intelligent display assembly offers the designer a choice of either 16 or 32 alphanumeric characters (the IDA 2416–16 and IDA 2416–32, respectively), and operates from just a +5 V supply. Based on the previously introduced DL 2416 four-character intelligent display, the IDA 2416 adds all the support logic required for direct connection to most microprocessor buses. The system interface takes place through a 26-pin connector, which has available on it the data and address lines as well as the control signals needed. Two additional connectors are included on the IDA 2416 – one of them is used for the power and ground connections, and the other is used to implement display enable selection.

System power requirements

Operating from a single +5 V power supply, the IDA 2416–16 requires a typical operating current of 450 mA with eight of the segments lit on each character. For the 32 character display, the current increases to 850 mA, typical. For the worst-case condition with all segments lit, the 16 character display draws 650 mA and the 32 character display requires 1250 mA. With the display blanked, the board circuitry draws about 70 mA.

Display interface

The display interface available on the 26-pin connector consists of seven data lines (DØ to D6), five address lines (AØ to A4), four display-enable lines ($\overline{DE1}$ to $\overline{DE4}$), several unused pins, and various control signals. All address, data, and control lines have either pull-up or pull-down 1 kΩ resistors.

$\overline{BL}$ (Blanking, active low): When this line is pulled low, it causes the entire IDA display to go blank without affecting the contents of the display memory on the DL 2416s. $\overline{BL}$ is active regardless of address or display enable lines. A flashing display can be realized by pulsing this line.

$\overline{WR}$ (Write, active low): To store a character in the display memory, this line must be pulsed low for a minimum of 200 ns. See timing diagram for timing and relationship to other signals. The $\overline{WR}$ input drives a Schmitt-trigger.

CUE (Cursor enable, active high): When high, this line permits the cursor to be displayed, and when brought low, it disables the cursor function without affecting the stored value. CUE is active regardless of address or display enable lines. A flashing cursor can be created by pulsing the CUE line low.

$\overline{CU}$ (Cursor select, active low): The cursor function (character with all segments lit) is loaded by selecting the digit address and holding $\overline{CU}$ true. A "1" on DØ writes the cursor. A "Ø" on DØ removes the cursor. The change occurs during the next write pulse per timing diagram.

$\overline{CLR}$ (Clear, active low): When held low for one display multiplex cycle (see DL 2416 data sheet for more information) of 15 ms, this line will cause all stored characters in the display, except for the cursor, to be cleared. $\overline{CLR}$ is active regardless of address or display enable lines. The $\overline{CLR}$ input drives a Schmitt-trigger.

$\overline{DE1}$ to $\overline{DE4}$ (Display enable, active low): There are four jumper selectable lines, any one of which can be selected to provide one of four board addresses that can be used when multiple IDAs are built into a system. When low, this line enables the selected display to permit data loading. The display enable input drives a Schmitt-trigger.

Address lines AØ to A4 are set up so that the right-most character is the lowest address. The left-most character is the highest address. Data lines are set up so that DØ is the least significant bit and D6 is the most significant bit.

Using the display interface

Through the use of memory-mapped I/O techniques, the IDA can be treated almost like a memory location – supply the data, address and proper control signals and the characters appear, with each character location independently addressable. The basic signal flow sequence to load a character would start with the address lines going to the desired address while the $\overline{CLR}$ and $\overline{BL}$ lines are high to permit the data to be loaded in and displayed. After the address has stabilized, the data can change to the desired values (including the cursor). After the data have stabilized, the $\overline{WR}$ pulse is started, and must remain low for at least 200 ns. Signals must be held stable for 75 ns, minimum, after the rising edge of the $\overline{WR}$ pulse to ensure correct loading, while the addresses must be stable for 650 ns preceding the same rising edge of the $\overline{WR}$ pulse. See the timing diagram for a pictorial explanation.

Enable selection

For board enable (the $\overline{DE1}$ through $\overline{DE4}$ lines) the user can choose any one of the four enable signals he has provided on the cable. This signal will be used to provide a master enable to each IDA. All that need be done is to insert the shorting plug in the appropriate position on the pins provided. This allows the user to make the system display the same information on two or more different IDAs or display different information on each of up to four groups of IDAs.

Optoelectronic characteristics at 25 °C

Maximum ratings

Supply voltage (V_{CC})	6.0 V
Voltage applied to any input	$-0.5 \ldots V_{CC} + 0.5$ V
Operating temperature	$-20 \ldots +65$ °C
Storage temperature	$-20 \ldots +70$ °C
Relative humidity at 65 °C (non-condensing)	85 %

DC characteristics

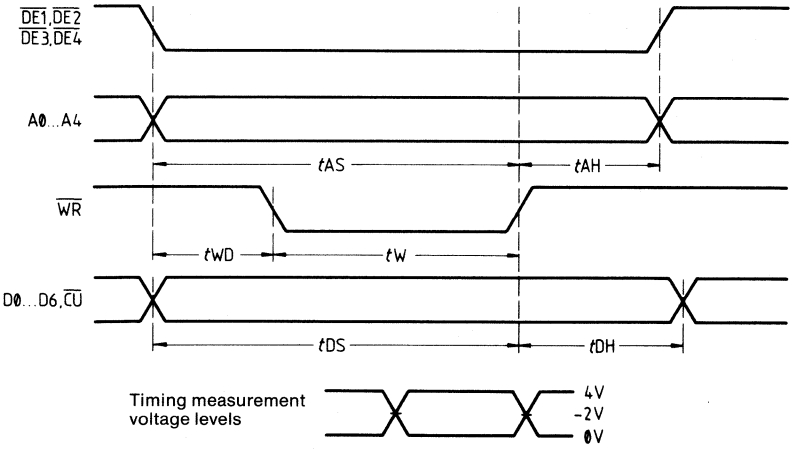
Symbol	Parameter	min.	typ.	max.	Unit	Test conditions
I_{CC}	V_{CC} supply current/digit		25		mA	V_{CC} = 5.0 V (8 segments/digit)
I_{CC}	V_{CC} supply current (total) (IDA 2416–16)			650	mA	V_{CC} = 5.0 V (all segments/digit)
I_{CC}	V_{CC} supply current (IDA 2416–32)			1250	mA	V_{CC} = 5.0 V (all segments/digit)
V_{CC}	Supply voltage	4.75	5.0	5.25	V	—
V_{IH}	Input voltage – high (all inputs)	2			V	V_{CC} = 5.0 V ±0.25 V
V_{IL}	Input voltage – low (all inputs)			0.8	V	V_{CC} = 5.0 V
I_{IH}	Input current – high (all inputs)			40	µA	V_{CC} = 5.5 V V_{IH} = 2.4 V
I_{IL}	Input current – low (all inputs)			2.2	mA	V_{CC} = 5.5 V V_{IL} = 0.4 V
I_V	Luminous intensity (Average per digit)		0.5		mcd	V_{CC} = 5.0 V (8 segments/digit)
λ_{peak}	Spectral peak wavelength		660		nm	—
	Viewing angle		±45		degrees	Vertical and horizontal from normal to display plane

Switching characteristics at 5 V and 25 °C (nanoseconds)

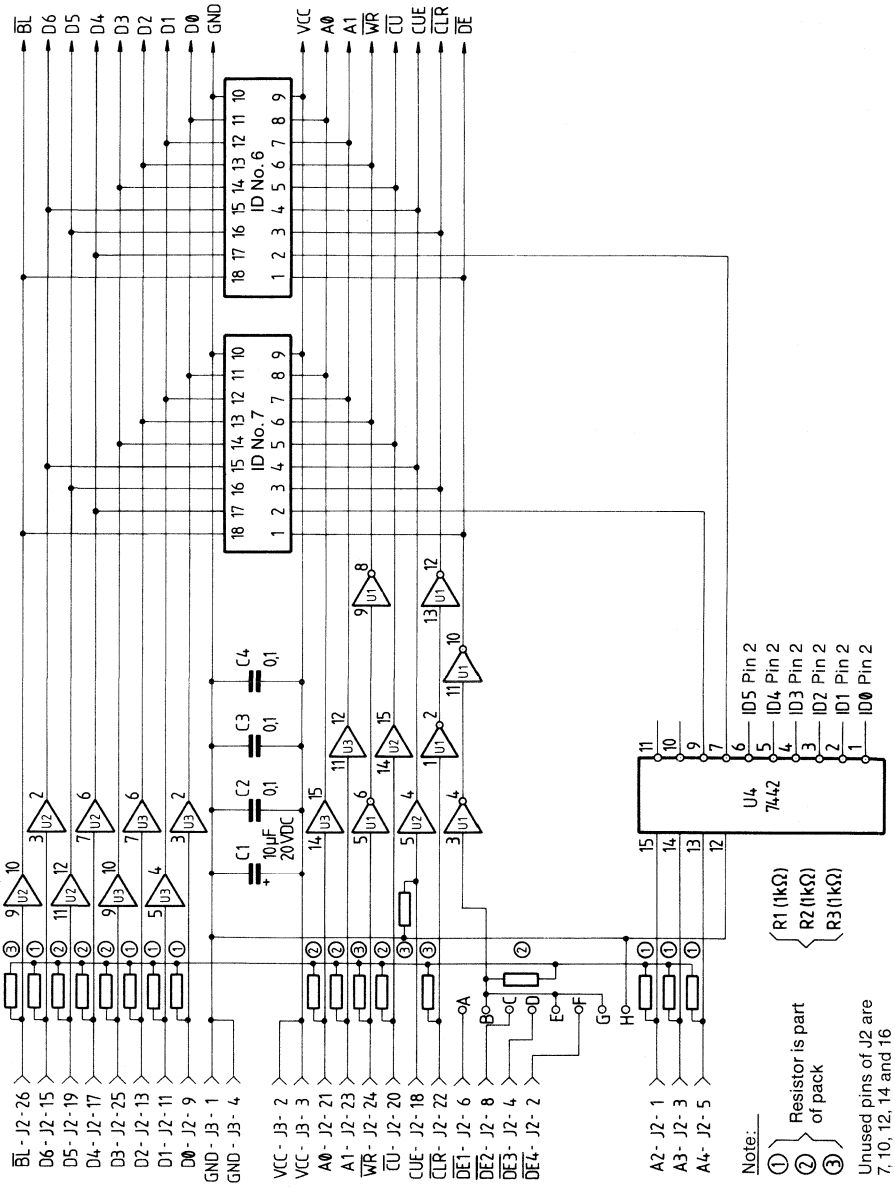
Symbol	Parameter	min.	Unit
*t*W	Write pulse	200	ns
*t*AS	Address/DE setup time	650	ns
*t*DS	Data setup time	650	ns
*t*WD	Write setup	200	ns
*t*DH	Data hold time	75	ns
*t*AH	Address/DE hold time	75	ns
*t*CLR	Clear time	15	ms

Timing characteristics

Write cycle waveforms



Internal block diagram



Alphanumeric intelligent display assembly with memory, decoder, and driver.
5.7 mm, red, 16, 20 or 32 digits, 16 segments plus decimal

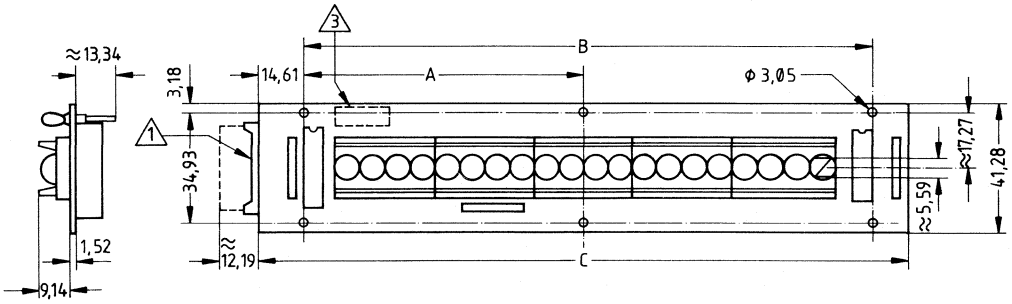
Features

- Complete alphanumeric display assembly utilizing the DL 3416
  - built-in multiplex and LED drive circuitry
  - built-in memory
  - built-in character generator
- Displays 64 character ASCII set
- Direct access to each digit independently
- Display blank function
- Memory clear function
- Cursor function
- Choice of 16, 20, or 32 character display length (other lengths optional)
- Single 5 V power supply
- TTL-compatible
- Easily interfaced to a microprocessor
- Schmitt-trigger inputs on data and write lines

Type	Ordering code	Description
IDA 3416–16	Q68000–A7239–F114	Single line 16 character display utilizing the DL 3416
IDA 3416–20	Q68000–A7242–F114	Single line 20 character display utilizing the DL 3416
IDA 3416–32	Q68000–A7164–F114	Single line 32 character display utilizing the DL 3416

Custom-specific lengths in increments of 4 characters upon request.

IDA 3416–16, IDA 3416–20

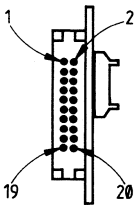


Dimensions in mm

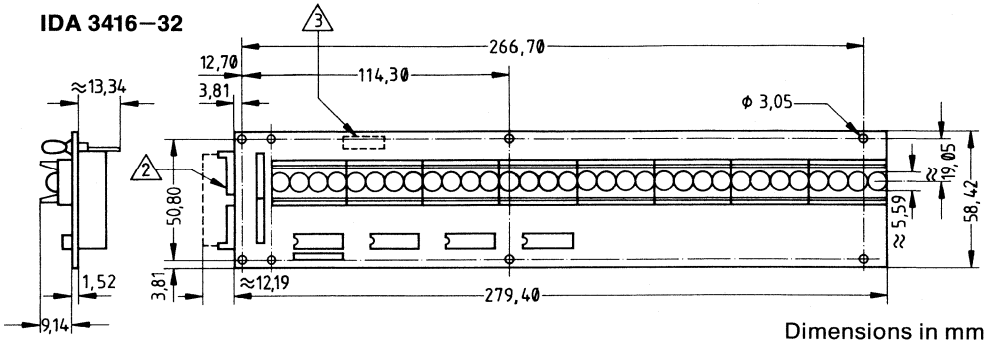
Type	A	B	C
IDA 3416–16	76.20	152.40	176.53
IDA 3416–20	92.71	185.42	209.55

Pin configuration of IDA 3416–16 and IDA 3416–20

Pin	Function	Pin	Function
J2–1	D6 Data line	J2–11	D1 Data line
J2–2	$\overline{BL}$ Blanking	J2–12	$\overline{CE2}$ Chip enable
J2–3	D5 Data line	J2–13	DØ Data line
J2–4	No connection	J2–14	$\overline{CU}$ Cursor select
J2–5	D4 Data line	J2–15	$\overline{WR}$ Write
J2–6	A1 Address line	J2–16	CUE Cursor enable
J2–7	D3 Data line	J2–17	A3 Address line
J2–8	AØ Address line	J2–18	No connection
J2–9	D2 Data line	J2–19	A4 Address line
J2–10	$\overline{CLR}$ Clear	J2–20	A2 Address line
J3–1	GND Ground	J3–3	V_{CC} Supply voltage
J3–2	V_{CC} Supply voltage	J3–4	GND Ground



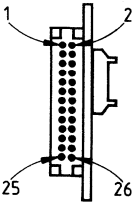
IDA 3416–32



Dimensions in mm

Pin configuration of IDA 3416–32

Pin	Function	Pin	Function
J2–1	A2 Address line	J2–14	No connection
J2–2	$\overline{DE4}$ Display enable	J2–15	D6 Data line
J2–3	A3 Address line	J2–16	No connection
J2–4	$\overline{DE3}$ Display enable	J2–17	D4 Data line
J2–5	A4 Address line	J2–18	CUE Cursor enable
J2–6	$\overline{DE1}$ Display enable	J2–19	D5 Data line
J2–7	No connection	J2–20	$\overline{CU}$ Cursor select
J2–8	$\overline{DE2}$ Display enable	J2–21	AØ Address line
J2–9	DØ Data line	J2–22	$\overline{CLR}$ Clear
J2–10	No connection	J2–23	A1 Address line
J2–11	D1 Data line	J2–24	$\overline{WR}$ Write
J2–12	No connection	J2–25	D3 Data line
J2–13	D2 Data line	J2–26	$\overline{BL}$ Blanking
J3–1	GND	J3–3	V_{CC}
J3–2	V_{CC}	J3–4	GND



Recommended mating connector

Connector	Function	Type	Suggested mfg.
⚠1 J2	Control/data	20 pin ribbon	BERG P/N 65496–007
⚠2 J2	Control/data	26 pin ribbon	BERG P/N 65484–011
⚠3 J3	Power	Molex	AMP P/N 1–87025–3 Housing P/N 87026–2

Optoelectronic characteristics at 25 °C

Maximum ratings

Supply voltage (V_{CC})	6.0 V
Voltage applied to any input	$-0.5 \ldots V_{CC} + 0.5$ V
Operating temperature	0 ... +65 °C
Storage temperature	−20 ... +70 °C

Optical characteristics (typical)

Luminous intensity (I_V) at V_{CC} = 5.0 V (average per digit) 8 segments/digit	0.8 mcd
Peak wavelength (λ_{peak})	660 nm
Viewing angle (φ) (vertical and horizontal from normal to display plane)	±40 degrees

DC characteristics at 25 °C

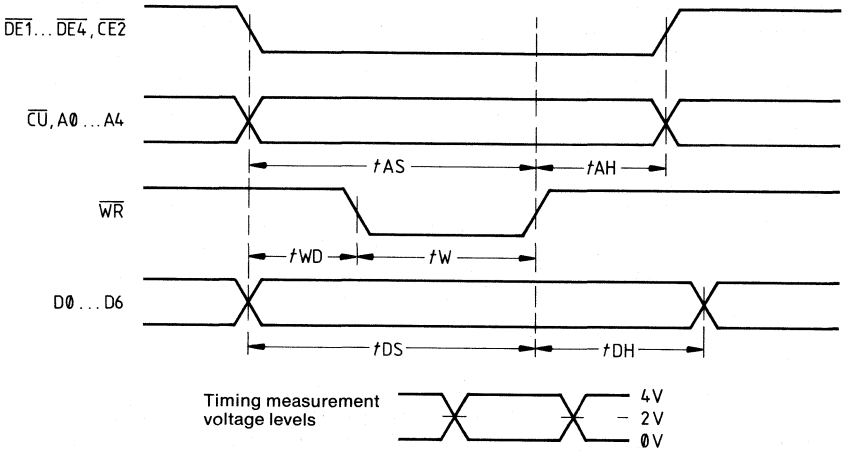
Symbol	Parameter	min.	typ.	max.	Test conditions
I_{CC}	V_{CC} supply current/digit (8 segments/digit)		25 mA		V_{CC} = 5.0 V
I_{CC}	V_{CC} supply current/digit (display blank)			6 mA	V_{CC} = 5.0 V; V_{IN} = Ø V $\overline{WR}$ = 5 V
I_{CC}	Total IDA 3416–16 (all segments/digit)			850 mA	V_{CC} = 5.0 V (see note 2)
I_{CC}	Total IDA 3416–20 (all segments/digit)			1050 mA	V_{CC} = 5.0 V (see note 2)
I_{CC}	Total IDA 3416–32 (all segments/digit)			1680 mA	V_{CC} = 5.0 V (see note 2)
V_{CC}	Supply voltage	4.75 V	5.0 V	5.25 V	
V_{IH}	Input voltage – high (all inputs)	3.5 V			V_{CC} = 5.0 V ±0.25 V
V_{IL}	Input voltage – low (all inputs)			0.8 V	V_{CC} = 5 V
I_{IH}	Input current – high (all inputs)			40 µA	V_{CC} = 5.5 V; V_{IN} = 2.4 V
I_{IL}	Input current – low (all inputs)			6.4 mA	V_{CC} = 5.5 V; V_{IN} = 0.4 V

Switching characteristics at 5 V and 25 °C (nanoseconds)

Symbol	Parameter	min.	Unit
*t*W	Write pulse	350	ns
*t*AS	Address setup	550	ns
*t*DS	Data setup	550	ns
*t*WD	Write delay	200	ns
*t*DH	Data hold	75	ns
*t*AH	Address hold	75	ns
*t*CLR	Clear	15	ms

Timing characteristics

Write cycle waveforms



Notes

1) For CMOS handling precautions see page 7.
2) Cursor should not be on any longer than 60 s
3) Cleaning solvents – do not use alcohol!

Description

The IDA 3416 series assembly is an extension of the very easy-to-use DL 3416 intelligent display. This product provides the designer with circuitry for display maintenance. It also minimizes interaction and interface normally required between the user's system and a multiplexed alphanumeric display.

The assembly consists of DL 3416s in a single row together with decoder and interface buffers on a single printed circuit board. Each DL 3416 provides its own memory, ASCII ROM character decoder, multiplexing circuitry, and drivers for its four 17-segment LEDs.

Intelligent display assemblies can be used for applications such as data terminals, controllers, instruments, and other products which require an easy-to-use alphanumeric display.

System overview

The intelligent display assembly offers the designer a choice of either 16, 20 or 32 alphanumeric characters and operates from just a +5 V supply. Based on the previously introduced DL 3416 four-character intelligent display, the IDA 3416 adds all the support logic required for direct connection to most microprocessor buses. The system interface takes place through a 20 or 26-pin connector, which has available on it the data and address lines as well as the control signals needed. One additional connector is used for the power and ground connections.

System power requirements

Operating from a single +5 V power supply, the IDA 3416 series assembly requires a typical operating current of 25 mA per digit with eight of the segments lit on each character. For the worst case condition with all segments lit, the current is 52 mA per digit and with the display blank the current is 6 mA per digit.

Display interface

The display interface available on the 20 or 26-pin connector consists of seven data lines (DØ to D6), five address lines (AØ to A4) and various control signals. All address, data, and control lines have either pull-up or pull-down 1 kohm resistors.

$\overline{BL}$ (Blanking, active low): When this line is pulled low, it causes the entire IDA display to go blank without affecting the contents of the display memory on the DL 3416s. $\overline{BL}$ is active regardless of address or display enable lines. A flashing display can be realized by pulsing this line.

$\overline{WR}$ (Write, active low): To store a character in the display memory, this line must be pulsed low for a minimum write time. See timing diagram for timing and relationships to other signals.

CUE (Cursor enable, active high): When high, this line permits the cursor to be displayed (see note 2, page 145), and when brought low, it disables the cursor function without affecting the stored value. CUE is active regardless of address or display enable lines. A flashing cursor can be created by pulsing the CUE line low.

$\overline{CU}$ (Cursor select, active low): The cursor function (character with all segments lit) is loaded by selecting the digit address and holding $\overline{CU}$ true. A "1" on DØ inserts the cursor. A "Ø" on DØ removes the cursor. The change occurs during a write pulse per the timing diagram.

$\overline{CLR}$ (Clear, active low): When held low for one display multiplex cycle (see DL 3416 data sheet for more information) of 15 ms, this line will cause all stored characters in the display, except for the cursor, to be cleared. $\overline{CLR}$ is active regardless of address or display enable lines.

$\overline{CE2}$ (Chip enable, active low): To store a character in the display memory, this line must be held low at least 550 nanoseconds preceding the leading edge of the $\overline{WR}$ pulse.

Address lines AØ to A4 are set up so that the right-most character is the lowest address. The left-most character is the highest address. Data lines are set up so that DØ is the least significant bit and D6 is the most significant bit.

Using the display interface

Through the use of memory-mapped I/O techniques, the IDA can be treated almost like a memory location – supply the data, address and proper control signals and the characters appear, with each character location independently addressable. The basic signal flow sequence to load a character would start with the address lines going to the desired address while the $\overline{CLR}$ and $\overline{BL}$ lines are high to permit the data to be loaded in and displayed. After the address has stabilized, the data can change to the desired values (including the cursor). After the data has stabilized, the $\overline{WR}$ pulse is started, and must remain low for at least 350 ns. Signals must be held stable for 75 ns, minimum, after the rising edge of the $\overline{WR}$ pulse to ensure correct loading, while the addresses must be stable for 550 ns preceding the same rising edge of the $\overline{WR}$ pulse. See the timing diagram for a pictorial explanation.

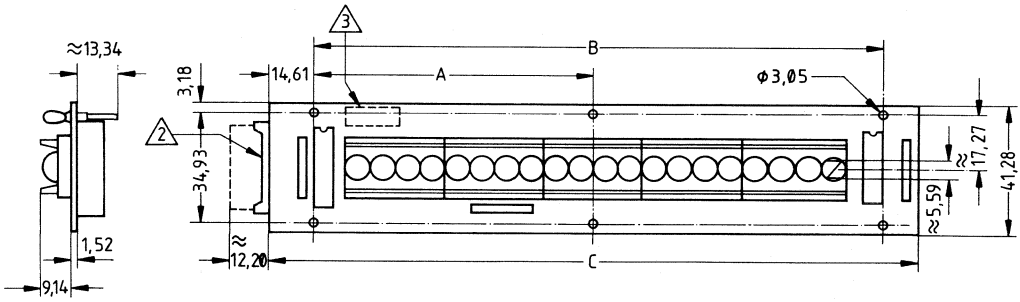
Alphanumeric intelligent display assembly with memory, decoder, and driver.
4.3/2.5 mm (nom.) upper and lower case letters, red, 16 or 20 digits, 22 segments

Features

- Complete alphanumeric display assembly utilizing the DL 3422
  - built-in multiplex and LED drive circuitry
  - built-in memory
  - built-in character generator
- Displays 96 character ASCII set
- Direct access to each digit independently
- Display blank function
- Memory clear function
- Cursor function
- Choice of 16 or 20 character display length (other lengths optional)
- Single 5.0 V power supply.
- TTL compatible
- Easily interfaced with a microprocessor
- Schmitt-trigger inputs on data and write lines

Type	Ordering code	Description
IDA 3422–16	Q68000–A7243–F114	Single line 16 character display utilizing the DL 3422
IDA 3422–20	Q68000–A7244–F114	Single line 20 character display utilizing the DL 3422

Custom-specific lengths in increments of 4 characters upon request.

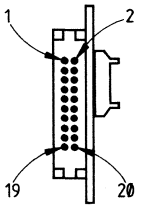


Dimensions in mm

Type	A	B	C
IDA 3422–16	76.20	152.40	176.53
IDA 3422–20	92.71	185.42	209.55

Pin configuration

Pin	Function	Pin	Function
J2–1	D6 Data line	J2–11	D1 Data line
J2–2	$\overline{BL}$ Blanking	J2–12	$\overline{CE2}$ Chip enable
J2–3	D5 Data line	J2–13	DØ Data line
J2–4	Unused	J2–14	$\overline{CU}$ Cursor select
J2–5	D4 Data line	J2–15	$\overline{WR}$ Write
J2–6	A1 Address line	J2–16	CUE Cursor enable
J2–7	D3 Data line	J2–17	A3 Address line
J2–8	AØ Address line	J2–18	Unused
J2–9	D2 Data line	J2–19	A4 Address line
J2–10	$\overline{CLR}$ Clear	J2–20	A2 Address line
J3–1	GND Ground	J3–3	V_{CC} Supply voltage
J3–2	V_{CC} Supply voltage	J3–4	GND Ground



Recommended mating connector

Connector	Function	Type	Suggested mfg.
⚠2 J2	Control/data	20 pin ribbon	BERG P/N 65496–007
⚠3 J3	Power	Molex	AMP P/N 1–87025–3 Housing P/N 87026–2

Optoelectronic characteristics at 25 °C

Maximum ratings

Supply voltage (V_{CC})	6.0 V
Voltage applied to any input	−0.5... V_{CC} +0.5 V
Operating temperature	0 ...+65 °C
Storage temperature	−20 ...+70 °C

Optical characteristics (typical)

Luminous intensity (I_V) at V_{CC} = 5.0 V (average per digit) 8 segments/digit	0.8 mcd
Peak wavelength (λ_{peak})	660 nm
Viewing angle (φ) (vertical and horizontal from normal to display plane)	±50 degrees

DC characteristics at 25 °C

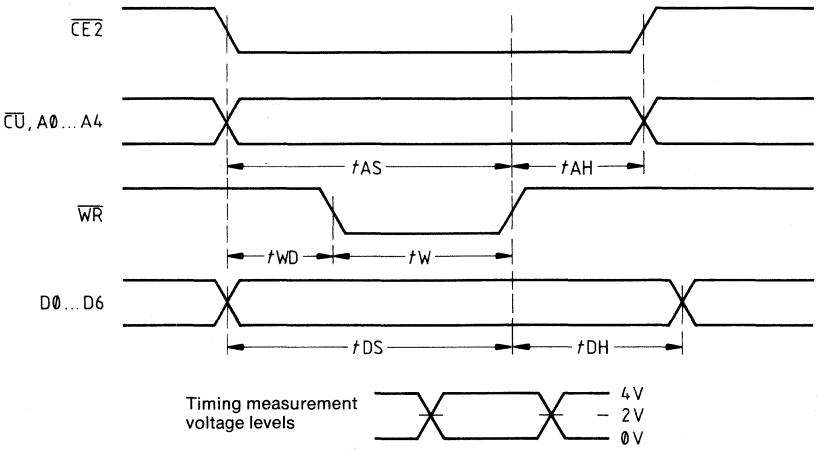
Symbol	Parameter	min.	typ.	max.	Test conditions
I_{CC}	V_{CC} supply current per digit (8 segments/digit)		20 mA		V_{CC} = 5.0 V
I_{CC}	V_{CC} supply current per digit (blank)			1 mA	V_{CC} = 5.0 V; V_{IN} = Ø V $\overline{WR}$ = 5 V
I_{CC}	Total IDA 3422–16 (all segments/digit)			640 mA	V_{CC} = 5.0 V (see note 2)
I_{CC}	Total IDA 3422–20 (all segments/digit)			800 mA	V_{CC} = 5.0 V (see note 2)
V_{CC}	Supply voltage	4.75 V	5.0 V	5.25 V	
V_{IH}	Input voltage – high (all inputs)	3.5 V			V_{CC} 5.0 V ±0.25 V
V_{IL}	Input voltage – low (all inputs)			0.8 V	V_{CC} = 5 V
I_{IH}	Input current – high (all inputs)			40 µA	V_{CC} = 5.5 V; V_{IN} = 2.4 V
I_{IL}	Input current – low (all inputs)			6.4 mA	V_{CC} = 5.5 V; V_{IN} = 0.4 V

Switching characteristics at 5 V and 25°C (nanoseconds)

Symbol	Parameter	min.	Units
*t*W	Write pulse	350	ns
*t*AS	Address setup	550	ns
*t*DS	Data setup	550	ns
*t*WD	Write delay	200	ns
*t*DH	Data hold	75	ns
*t*AH	Address hold	75	ns
*t*CLR	Clear	15	ms

Timing characteristics

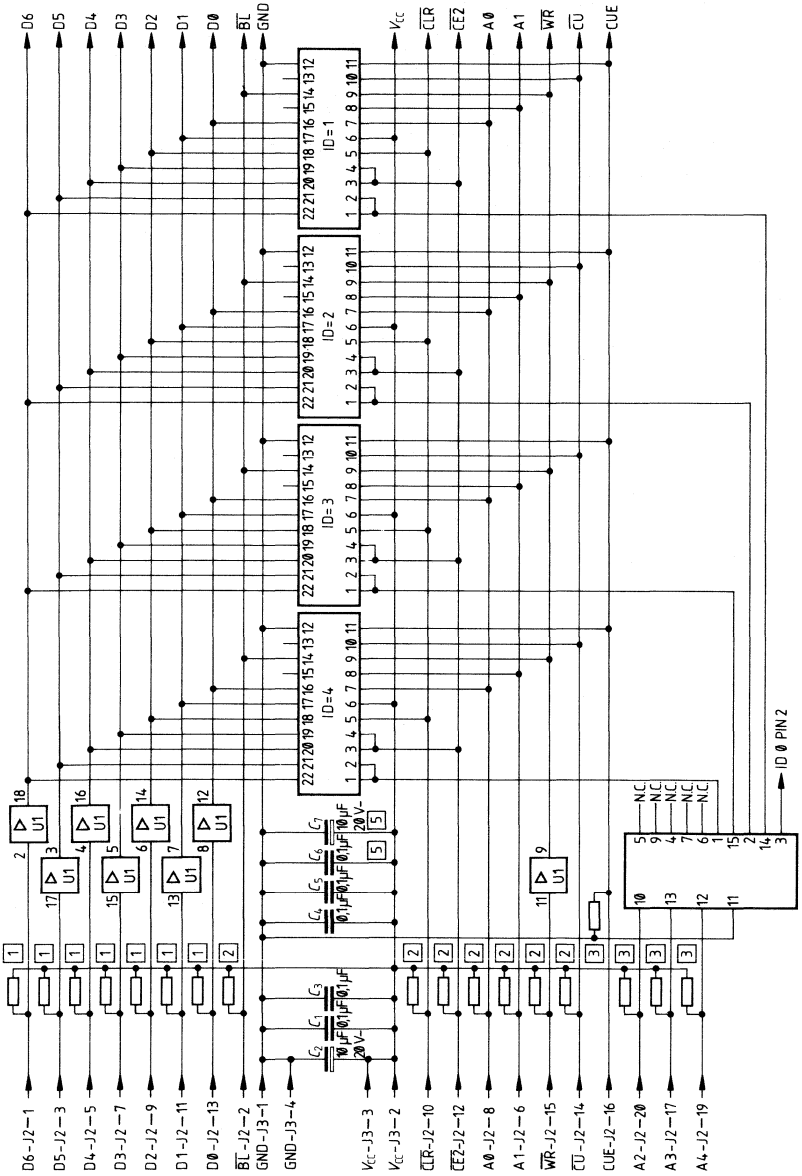
Write cycle waveforms



Notes

1) For CMOS handling precautions see page 7
2) Cursor should not be on any longer than 60 s
3) Cleaning solvents – do not use alcohol!

Internal block diagram



1 Part of resistor pack RP 1
2 Part of resistor pack RP 2
3 Part of resistor pack RP 3
4 Unused pins of J2 are 4 and 18
5 Used on 3422 – 20 only

Description

The IDA 3422 series assembly is an extension of the very easy-to-use DL 3422 intelligent display. This product provides the designer with circuitry for display maintenance. It also minimizes interaction and interface normally required between the user's system and a multiplexed alphanumeric display.

The assembly consists of DL 3422s in a single row together with decoder and interface buffers on a single printed circuit board. Each DL 3422 provides its own memory, ASCII ROM character decoder, multiplexing circuitry, and drivers for its four 22-segment LEDs.

Intelligent display assemblies can be used for applications such as data terminals, controllers, instruments, and other products which require an easy to use alphanumeric display.

System overview

The intelligent display assembly offers the designer a choice of either 16 or 20 alphanumeric characters and operates from just a +5 V supply. Based on the previously introduced DL 3422 four-character intelligent display, the IDA 3422 adds all the support logic required for direct connection to most microprocessor buses. The system interface takes place through a 20-pin connector, which has available on it the data and address lines as well as the control signals needed. One additional connector is used for the power and ground connections.

System power requirements

Operating from a single +5 V power supply, the IDA 3422 series assembly requires a typical operating current of 20 mA per digit with eight of the segments lit on each character. For the worst case condition with all segments lit, the current is 40 mA per digit and with the display blank the current is 1 mA per digit.

Display interface

The display interface available on the 20-pin connector consists of seven data lines (DØ to D6), five address lines (AØ to A4), two unused pins, and various control signals. All address, data, and control lines have either pull-up or pull-down 1 kohm resistors.

$\overline{BL}$ (Blanking, active low): When this line is pulled low, it causes the entire IDA display to go blank without affecting the contents of the display memory on the DL 3422s. $\overline{BL}$ is active regardless of address or display enable lines. A flashing display can be realized by pulsing this line.

$\overline{WR}$ (Write, active low): To store a character in the display memory, this line must be pulsed low for a minimum write time. See timing diagram for timing and relationships to other signals.

CUE (Cursor enable, active high): When high, this line permits the cursor to be displayed (see note 2, page 152), and when brought low, it disables the cursor function without affecting the stored value. CUE is active regardless of address or display enable lines. A flashing cursor can be created by pulsing the CUE line low.

$\overline{CU}$ (Cursor select, active low): The cursor function (character with all segments lit) is loaded by selecting the digit address and holding $\overline{CU}$ true. A "1" on DØ inserts the cursor. A "Ø" on DØ removes the cursor. The change occurs during a write pulse per the timing diagram.

$\overline{CLR}$ (Clear, active low): When held low for one display multiplex cycle (see DL 3422 data sheet for more information) of 15 ms, this line will cause all stored characters in the display, except for the cursor, to be cleared. $\overline{CLR}$ is active regardless of address or display enable lines.

$\overline{CE2}$ (Chip enable, active low): To store a character in the display memory, this line must be held low at least 550 nanoseconds preceding the leading edge of the $\overline{WR}$ pulse.

Address lines AØ to A4 are set up so that the right-most character is the lowest address. The left-most character is the highest address. Data lines are set up so that DØ is the least-significant bit and D6 is the most-significant bit.

Using the display interface

Through the use fo memory-mapped I/O techniques, the IDA can be treated almost like a memory location – supply the data, address and proper control signals and the characters appear, with each character location independently addressable. The basic signal flow sequence to load a character would start with the address lines going to the desired address while the $\overline{CLR}$ and $\overline{BL}$ lines are high to permit the data to be loaded in and displayed. After the address has stabilized, the data can change to the desired values (including the cursor). After the data have stabilized, the $\overline{WR}$ pulse is started, and must remain low for at least 350 ns. Signals must be held stable for 75 ns, minimum, after the rising edge of the $\overline{WR}$ pulse to ensure correct loading, while the addresses must be stable for 550 ns preceding the same rising edge of the $\overline{WR}$ pulse. See the timing diagram for a pictorial explanation.

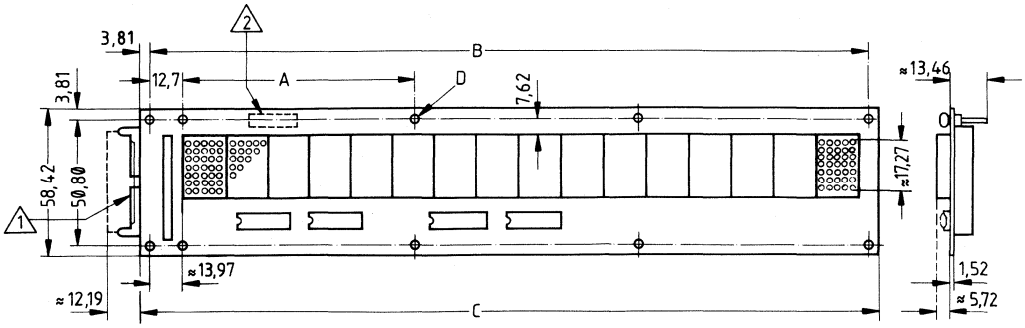
Alphanumeric intelligent dot-matrix display assembly

17.3 mm, 5×7 dot matrix, 16 and 20 digits
Emission colors: orange, green

Features

- Complete alphanumeric display assembly utilizing the DLX 713 * series 5×7 dot matrix display
  - built-in multiplex and LED drive circuitry
  - built-in memory
  - built-in character generator
- Displays 96 character ASCII set, including both upper and lower case characters
- Direct access to each digit independently
- Three brightness levels
- Display blank function
- Lamp test function
- Wide viewing angle, ±75 degrees
- Readable in high ambient lighting
- Available in orange and green
- Choice of 16 or 20 character display lengths
- Single 5 V power supply
- Easily interfaced with a microprocessor
- TTL-compatible
- Fully buffered inputs

Type	Color	Ordering code	Description
IDA 7135–16	orange	Q68000–A6385–F114	Single line, 16 character, utilizing the DLO 7135
IDA 7137–16	green	Q68000–A6389–F114	Single line, 16 character, utilizing the DLG 7137
IDA 7135–20	orange	Q68000–A6386–F114	Single line, 20 character, utilizing the DLO 7135
IDA 7137–20	green	Q68000–A6390–F114	Single line, 20 character, utilizing the DLG 7137



Dimensions in mm:

	A	B	C	D
IDA 7135–16 IDA 7137–16	typ. 96.52	302.26	306.07	10 digits typ. 3.05
IDA 7135–20 IDA 7137–20	typ. 90.17	373.38	377.19	12 digits typ. 3.94

Pin configuration

Pin	Function		Pin	Function	
J2–1	A2	Address line	J2–14		No connection
J2–2		No connection	J2–15	D6	Data line
J2–3	A3	Address line	J2–16		No connection
J2–4		No connection	J2–17	D4	Data line
J2–5	A4	Address line	J2–18	$\overline{BL1}$	Brightness
J2–6		No connection	J2–19	D5	Data line
J2–7		No connection	J2–20		No connection
J2–8		No connection	J2–21	AØ	Address line
J2–9	DØ	Data line	J2–22	$\overline{BLØ}$	Brightness
J2–10		No connection	J2–23	A1	Address line
J2–11	D1	Data line	J2–24	$\overline{WR}$	Write
J2–12		No connection	J2–25	D3	Data line
J2–13	D2	Data line	J2–26	$\overline{LT}$	Lamp test
J3–1	GND	Ground	J3–3	V_{CC}	Supply voltage (+5 V)
J3–2	V_{CC}	Supply voltage (+5 V)	J3–4	GND	Ground

Optoelectronic characteristics at 25 °C

Maximum ratings

Supply voltage (V_{CC})	6.0 V
Voltage applied to any input	$-0.5 \ldots V_{CC} + 0.5$ V
Operating temperature	0 ... +65 °C
Storage temperature	−20 ... +65 °C
Relative humidity at 65 °C (non-condensing)	85 %

Optical characteristics (typical)

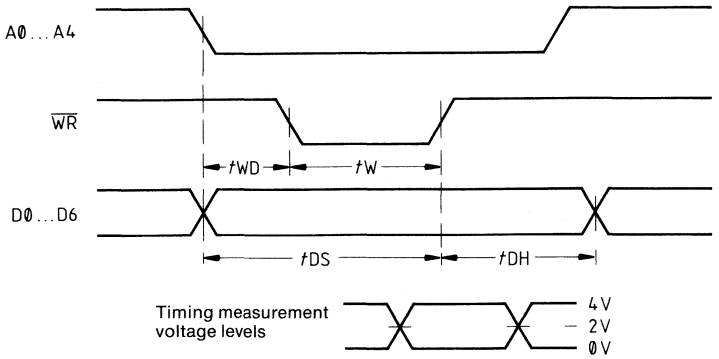
Luminous intensity/dot (average) at V_{CC} = 5 V:	
IDA 7135	500 µcd
IDA 7137	500 µcd
Digit size	17.27 mm
Viewing angle	±75 degrees
Spectral peak wavelength:	
IDA 7135 (orange)	630 nm
IDA 7137 (green)	565 nm

DC characteristics

Symbol	Parameter	min.	typ.	max.	Test conditions
V_{CC}	Supply voltage	4.75 V		5.25 V	
I_{CC}	V_{CC} supply current/digit		170 mA	220 mA	$\overline{BL0}$ = 1, $\overline{BL1}$ = 1, V_{CC} = 5.0 V
I_{CC}	V_{CC} supply current/digit		85 mA		$\overline{BL0}$ = Ø, $\overline{BL1}$ = 1, V_{CC} = 5.0 V
I_{CC}	V_{CC} supply current/digit		42 mA		$\overline{BL0}$ = 1, $\overline{BL1}$ = Ø, V_{CC} = 5.0 V
I_{CC}	V_{CC} supply current/digit (blank)		5 mA	10 mA	$\overline{BL0}$ = Ø, $\overline{BL1}$ = Ø, V_{CC} = 5.0 V
I_{IL}	Input current – low			160 µA	V_{CC} = 5.0 V
V_{IL}	Input voltage – low (all inputs)			1.0 V	V_{CC} = 5.0 V
V_{IH}	Input voltage – high (all inputs)	2.7 V			V_{CC} = 5.0 V ± 0.25 V

Timing characteristics

Write cycle waveforms



Switching characteristics at 5 V and 25 °C (nanoseconds)

Symbol	Parameter	min.	Units
*t*W	Write pulse	200	ns
*t*DS	Data setup time	230	ns
*t*DH	Data hold time	100	ns
*t*WD	Write delay	30	ns

Character set

D3...D0 / D6...D4	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
000 001	Blanked characters															
010		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
011	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
100	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
101	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
110	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
111	p	q	r	s	t	u	v	w	x	y	z	{	|	}	~	

Description

The IDA 713* series assembly is an extension of the single character DLX 713*, 5×7 fully intelligent dot matrix display. This display assembly provides the designer with circuitry for display maintenance, while minimizing the interaction and interface normally required between the user's system and a multiplexed alphanumeric display.

Intelligent display assemblies can be used for applications such as P.O.S. terminals, message systems, industrial equipment, instrumentation, and any other products requiring a large, easily readable, "user friendly", alphanumeric display.

System overview

The intelligent display assembly offers the designer a choice of either 16 (IDA 713*–16) or 20 (IDA 713*–20) alphanumeric characters. Based on the DLX 713* intelligent dot matrix display, the IDA 713* adds all the support logic required for direct connection to most microprocessor buses. The system interface takes place through a 26 pin connector, which has the data and address lines as well as the control signals available. One additional connector is used for the power and ground connections.

System power requirements

Operating from a single +5 V power supply, the IDA 713*–16 requires a typical operating current of 2720 mA at brightest level. For the 20 character assembly, typical operating current is 3400 mA. For worst case conditions, the 16 character assembly draws 3520 mA and the 20 character assembly draws 4400 mA. With the display blanked, the board circuitry for the 16 character assembly draws 80 mA, and the 20 character assembly draws 100 mA.

Display interface

The display interface available on the 26 pin connector consists of seven data lines (DØ to D6), five address lines (AØ to A4), two brightness inputs ($\overline{BL0}$ to $\overline{BL1}$), lamp test ($\overline{LT}$), and the write line ($\overline{WR}$). All address and data lines have 1 kohm pull-up resistors.

$\overline{BL0}$ and $\overline{BL1}$ (Brightness, active low): When both of these are pulled low, it causes the entire IDA display to go blank without affecting the contents of the display memory on the DLX 713*'s. $\overline{BLX}$ is active regardless of address or display enable lines. These two lines are used to vary the intensity of the display to one of four levels.

$\overline{WR}$ (Write, active low): To store a character in the display memory, this line must be pulsed low for a minimum of 200 ns. See timing diagram for timing and relationships to other signals.

$\overline{LT}$ (Lamp test, active low): This line can be pulsed to light all displays dots.

Using the display interface

Through the use of memory-mapped I/O techniques, the IDA can be treated almost like a memory location – supply the data, address and proper control signals and the characters appear, with each character location independently addressable. The basic signal flow sequence to load a character would start with the address lines going to the desired address. After the address has stabilized, the data can change to the desired values. After the data have stabilized, the $\overline{WR}$ pulse is started, to ensure correct loading. See the timing diagram for a pictorial explanation.

Lamp test

The lamp test ($\overline{LT}$) when activated causes all dots on the display to be illuminated at half brightness. The lamp test function is independent of write ($\overline{WR}$) and the settings of the blanking inputs ($\overline{BL0}$, $\overline{BL1}$).

This convenient test gives a visual indication that all dots are functioning properly. Lamp test may also be used as a cursor function or pointer which does not destroy previously displayed characters.

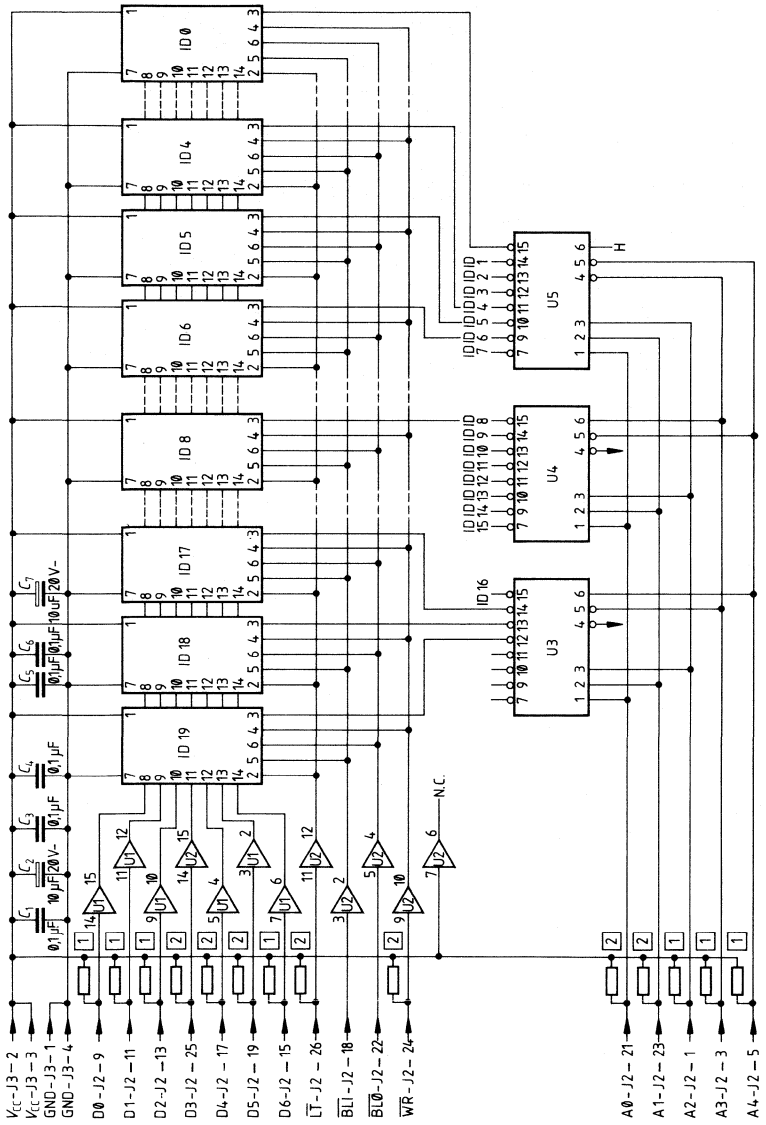
Dimming and blanking the display

Brightness level	$\overline{BL1}$	$\overline{BL0}$
Blank	0	0
¼ brightness	0	1
½ brightness	1	0
Full brightness	1	1

Recommended mating connector

Connector	Function	Type	Suggest mfg.
⚠1 J2	Control/data	26-pin ribbon	BERG P/N 65948–011
⚠2 J3	Power	Molex	AMP P/N 87066–4

Internal block diagram



Note: 1 Part of resistor pack RP1 (IK SIP)
2 Part of resistor pack RP2 (IK SIP)

Summary of Types/Ordering Codes

Summary of types (alphanumeric)		Page
DL 1414	Q68000-A5559-F114	11
DL 1416	Q68000-A4825-F114	28
DL 1814	Q68000-A7156-F114	54
DL 2416	Q68000-A5577-F114	60
DL 2416 H	Q68000-A6365-F114	60
MDL 2416	Q68000-A7219-F114	68
MDL 2416 B	Q68000-A7309-F114	68
DL 3416	Q68000-A6366-F114	88
DL 3416 H	Q68000-A6367-F114	88
DL 3422	Q68000-A6378-F114	96
DLO 7135	Q68000-A7157-F114	104
DLG 7137	Q68000-A7159-F114	104
IDA 1414-16-1	Q68000-A6380-F114	120
IDA 1414-16-2	Q68000-A6381-F114	120
IDA 1416-32	Q68000-A6382-F114	127
IDA 2416-16	Q68000-A6375-F114	134
IDA 2416-32	Q68000-A6376-F114	134
IDA 3416-16	Q68000-A7239-F114	141
IDA 3416-20	Q68000-A7242-F114	141
IDA 3416-32	Q68000-A7164-F114	141
IDA 3422-16	Q68000-A7243-F114	149
IDA 3422-20	Q68000-A7244-F114	149
IDA 7135-16	Q68000-A6385-F114	157
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Q68000-A5559-F114	DL 1414	11
Q68000-A5577-F114	DL 2416	60
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Q68000-A6366-F114	DL 3416	88
Q68000-A6367-F114	DL 3416 H	88
Q68000-A6375-F114	IDA 2416-16	134
Q68000-A6376-F114	IDA 2416-32	134
Q68000-A6378-F114	DL 3422	96
Q68000-A6380-F114	IDA 1414-16-1	120
Q68000-A6381-F114	IDA 1414-16-2	120
Q68000-A6382-F114	IDA 1416-32	127
Q68000-A6385-F114	IDA 7135-16	157
Q68000-A6386-F114	IDA 7135-20	157
Q68000-A6389-F114	IDA 7137-16	157
Q68000-A6390-F114	IDA 7137-20	157
Q68000-A7156-F114	DL 1814	54
Q68000-A7157-F114	DLO 7135	104
Q68000-A7159-F114	DLG 7137	104
Q68000-A7164-F114	IDA 3416-32	141
Q68000-A7219-F114	MDL 2416	68
Q68000-A7239-F114	IDA 3416-16	141
Q68000-A7242-F114	IDA 3416-20	141
Q68000-A7243-F114	IDA 3422-16	149
Q68000-A7244-F114	IDA 3422-20	149
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